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COORDINATED SCIENCE LABORATORY

PROGRESS REPORT FOR THE JOINT SERVICES ELECTRONICS PROGRAM

FOR THE PERIOD
1 APRIL 1990 THROUGH 31 MARCH 1991
FOR
GRANT N00014-90-J-1270

UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

UNCLASSIFIED

CURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS None
2a. SECURITY CLASSIFICATION AUTHORITY 2b. DECLASSIFICATION / DOWNGRADING SCHEDULE	3. DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION Coordinated Science Lab University of Illinois 6b. OFFICE SYMBOL (If applicable) N/A	7a. NAME OF MONITORING ORGANIZATION Office of Naval Research
6c. ADDRESS (City, State, and ZIP Code) 1101 W. Springfield Ave. Urbana, IL 61801	7b. ADDRESS (City, State, and ZIP Code) Arlington, VA 22217
8a. NAME OF FUNDING / SPONSORING ORGANIZATION Joint Services Electronics Program 8b. OFFICE SYMBOL (If applicable) N/A	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER N00014-90-J-1270
8c. ADDRESS (City, State, and ZIP Code) Arlington, VA 22217	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO / WORK UNIT ACCESSION NO

11. TITLE (Include Security Classification)
Second Annual Progress Report

12. PERSONAL AUTHOR(S)
Jenkins, W. K. (Principal Investigator)

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Progress	FROM 4/1/90 TO 3/31/91	6/30/91	105

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This is the second annual progress report of the research conducted at the Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, under the sponsorship of the Joint Services Electronics Program from 1 April 1990 through 31 March 1991. The research areas include: (1) Physical Electronics, (2) VLSI Circuits and Computer Systems, (3) Electronic Systems, and (4) Management Initiatives (discretionary Director's unit). This report summarizes the areas of research, identifies the most significant results, and lists the publications sponsored by JSEP as well as other sponsoring agencies.

20. DISTRIBUTION / AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION Unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code) / 22c. OFFICE SYMBOL

DD Form 1473, JUN 86 Previous editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE

UNCLASSIFIED

JSEP ANNUAL PROGRESS REPORT

For the Period

1 April 1990 through 31 March 1991

Joint Services Electronics Program
Grant N00014-90-J-1270

Monitored by the
Office of Naval Research

William Kenneth Jenkins
JSEP Principal Investigator
Coordinated Science Laboratory

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EXECUTIVE SUMMARY

I. Summary of the Program

The current JSEP grant at the Coordinated Science Laboratory runs from October 1, 1989 through September 30, 1992. This report covers the period from April 1, 1990 through March 31, 1991, which is the second half of the first year and the first half of the second year. This six-month offset reporting period, which has been used consistently during the past few years, is necessitated by the timing of the annual review relative to the October 1 start date of the JSEP fiscal year.

The Illinois JSEP program is directed by Professor W. K. Jenkins, who holds a joint appointment as Director of the Coordinated Science Laboratory and Professor of Electrical and Computer Engineering. The Director is advised on both technical and managerial issues by the JSEP Internal Advisory Committee, which consists of individuals who represent different technical areas of the JSEP program. Professor Karl Hess is currently serving as the advisor for Physical Electronics, Professor Michael Pursley for Electronic Systems, and Professor Timothy Trick for VLSI Circuits and Computer Systems. Professor Trick's participation also provides coordination with the Electrical and Computer Engineering Department (ECE) and the faculty in the Microelectronics and Gaseous Electronics Laboratories, which is helpful to ECE faculty who participate in the JSEP program but who are not full-time residents of the CSL building. Professor Hess's participation on the JSEP Internal Advisory Committee provides a similar coordination with research activities in the Beckman Institute, which also houses the laboratories of some of the JSEP senior investigators.

The Illinois JSEP program consists of eighteen research units that are organized into four major areas: (1) Physical Electronics, (2) VLSI Circuits and Computer Systems, (3) Electronic Systems, and (4) the Director's Research Initiatives. Each unit is described briefly below and the Scientific Objectives and Summary of Progress for each are presented in the body of this report. Requests for additional information and/or technical publications resulting from the JSEP program should be directed to Professor W. K. Jenkins, Coordinated Science Laboratory, 1101 W. Springfield Avenue, Urbana, IL 61801.

Physical Electronics

Unit 1 is the project directed by Professor J. Greene on low-energy ion/surface interactions during metal and semiconductor crystal growth from the vapor phase. This work, a continuation of Professor Greene's previous work on the JSEP program, currently is progressing on schedule with overall scope and level of effort remaining consistent with the original three-year proposal. Professor Greene was recently named winner of the Swedish Erlangër Award for his contributions to the field of thin film physics. While this prestigious award was presented to Professor Greene for his total contributions that go well beyond the work he has done on the JSEP program, JSEP support played a key role in having fostered his research programs in their early days, as well as providing sustained support over a long period of time.

In Unit 2 Professors K. Hess and U. Ravaioli continue to expand the science of computational electronics for semiconductor devices. They are engaged in a new effort to merge Monte Carlo methods and hydrodynamic models to provide a higher degree of sophistication to device simulation. This research is conducted within the Beckman Institute, where Professor Hess now serves as Director of the Computational Electronics Center, formed several years ago under NSF sponsorship. The facilities provided in the Beckman Institute by this NSF center, and also by the NSF National Center for Supercomputing Applications (NCSA), have greatly enhanced the JSEP research conducted within this environment. Professor Ravaioli was recently promoted to Associate Professor and now serves as a regular member of the JSEP research team.

Professor K. Cheng continues to work with Professor G. Stillman on Unit 3 in researching new studies for gas source MBE/CBE for optoelectronic devices. Professor Cheng, who was recently appointed to the rank of Associate Professor with tenure, now operates two MBE chambers as part of his normal research activities. One chamber is located in the Electrical Engineering Research Laboratory, while the second is located in CSL and operates as one of the seven interconnected chambers in the EpiCenter. In 1990 Professor Gregory Stillman was chosen by the Awards Committee of the 17th Gallium Arsenide Symposium as the recipient of the 1990 Symposium Award

and the Heinrich Welker Memorial Medal for his outstanding contributions to gallium arsenide device technology. The JSEP program has provided long-term support for Professor Stillman's work in this area and, therefore, has contributed substantially to his recently acknowledged accomplishments.

Professor J. Coleman (Unit 4) has undertaken new work in heterostructure electronic devices by MOCVD technology. He up-graded his MOCVD system recently when he moved into the new Microelectronics Laboratory. Last year a portion of the JSEP Director's Fund was used to help fund some of Professor Coleman's new MOCVD equipment. Presently, the research on this unit is progressing on schedule and with the level of support that was proposed in the original three-year proposal.

In Unit 5, Professors J. Lyding and J. Tucker continue to use Lyding's patented scanning tunneling microscope (STM) for the characterization of semiconductor heterolayers and devices. The superb imaging capability of the newly developed scanning tunneling microscope allows experimental investigations of heterolayers that were not previously possible. The construction of a new ultra-high vacuum STM was completed recently, which allows the probing of properties of III-V heterolayers on a nanometer scale. Recent results of this work are cited in Section II under JSEP Significant Accomplishments.

Due to the high-risk nature of the research in Unit 6 to develop a reproducible semiconductor frequency standard with devices based on rare earth ions incorporated into III-V materials, it was decided at the end of the first year that this unit would be reduced in scope and brought to a conclusion by the end of the second year. During the second year, efforts have been devoted to carrying out femtosecond laser measurements on erbium-doped semiconductors that were obtained from researchers at Wright-Patterson Air Force Base in Dayton, Ohio.

Unit 7 began as a cooperative effort among Professors I. Adesida, J. Kolodzey, and J. P. Leburton, although Professor Kolodzey has recently left the University and the unit is now continued by Professors Adesida and Leburton. This unit addresses problems of electronic and transport properties of ultra-low-dimensional semiconductor structures. This research represents a

team approach, with J. P. Leburton providing important theoretical expertise and I. Adesida providing experimental expertise. This unit has already made important advances in the conception and verification of a new tunneling mechanism in MODFET structures and, as such, was cited as one of the most significant accomplishments of the previous JSEP contract.

In Unit 8 Professor R. Mittra is working with Assistant Professor J. Schutt-Aine on a project in electromagnetic modeling and simulation of high-speed digital circuit interconnections. They continue efforts to develop a better understanding of the behavior and performance of interconnections in microelectronic packaging and high-speed digital network applications. Although this work is essentially in electromagnetics, it has been grouped with the Physical Electronics area to emphasize its importance in high-speed devices.

VLSI Circuits and Computer Systems

Units 9 and 10 support the work of Professors Patel, Hwu, Banerjee, Fuchs, and Iyer of the Center for Reliable and High-Performance Computing at CSL. Unit 9 addresses important problems in high-performance computer architectures, with J. Patel and W.-M. Hwu serving as the senior investigators. They continue to develop, model, and analyze efficient, high-performance computer architectures that exploit both high-density and high-speed semiconductor technologies. Professors Banerjee, Fuchs, and Iyer conduct the research of Unit 10 on fault-tolerant parallel computer systems. They continue to research concepts in reliable computing that will provide an understanding of the basic principles in design and analysis of reliable VLSI-based parallel computer architectures.

The research in Unit 11 has been conducted by Professors F. Preparata, M. Loui, and B. Wah on the analysis and design of efficient computation techniques, with the dominant theme being parallel computation that leads to suitable structures in VLSI. In January 1991, Professor Preparata retired from the University and Professor D. Brown joined the unit to help supervise the continuing graduate students and to provide much needed expertise in computation theory in the areas of parallel algorithms and multiprocessor machine architectures. Note that emphasis in this unit is on the

development, analysis, and design of efficient structures (algorithms), whereas the emphasis in Units 9 and 10 is on machine design and machine architecture.

The research in Unit 12 on computer-aided design of very high-speed integrated circuits is conducted by Professors I. Hajj, S. Kang, and V. Rao. The objective of their work is to develop analysis and design techniques for reliable high-speed integrated circuit designs. This includes the automatic synthesis of testable circuits with a reduced number of devices, automatic generation of layout using two metal interconnects, and the development of mathematical methods and algorithms for optimizing the design. The work of this unit has produced the fast timing and reliability simulator, ILLIADS-R, which is cited as one of this year's JSEP Outstanding Accomplishments in Section II.

Electronic Systems

Units 13 and 14 are research projects in the control systems area. During the reporting period, Professors Kokotovic, Kumar, and Poolla conducted the research in Unit 13, which seeks to develop a fundamental understanding of how to design high-performance and robust adaptive systems for use in control, filtering, estimation, and identification. In particular, they have been studying important issues concerning the fundamental behavior of least squares parameter estimators (such as stability and convergence) and self-tuning properties and robustness of adaptive systems. In April 1991 Professor Kokotovic retired from the University, and this research is now continued by Professors Kumar and Poolla and their research assistants. In recognition of his outstanding professional contributions in the field, Professor Kokotovic was recently awarded the Georgio Quazza Medal of the International Federation of Automatic Control, the highest recognition from IFAC. He was also named the Hendrik Bode Lecturer for the IEEE Decision and Control Conference to be held in Brighton, England in 1991. JSEP support was instrumental in sustaining Professor Kokotovic's research programs over much of his 25-year career at the Coordinated Science Laboratory.

The research of Unit 14 on decentralized and distributed control of large dynamic systems is conducted by Professors T. Başar, J. Medanic, and W. Perkins. This work has applications to

aircraft control, ship steering, vibration control of large flexible space structures, and remote control and navigation of all-terrain vehicles.

Professors Y. Bresler, T. Huang, and D. Munson are the senior investigators on Unit 15, which is a study of sensor-array imaging techniques for dynamic scenes. This work in signal processing has important applications in synthetic aperture radar (SAR), X-ray computer tomography (CT), and scanning laser range finders, to name a few. The objective is to study basic issues in using sensor arrays to image dynamic scenes, particularly ones in which the amount of object motion or scene change is significant during the time interval used to collect each image frame. Professor Y. Bresler was recently awarded a Presidential Young Investigator Award by the National Science Foundation.

In Unit 16 Professors B. Hajek, M. Pursley, and D. Sarwate are researching topics in survivable communication networks. Their objective is to improve the state of the art by investigating critical issues in communication network design and performance. In particular, they seek a better understanding of the fundamental trade-offs between communication efficiency and survivability. They are working with improved modulation and coding schemes, receiver processing techniques, and network protocols for use in communication networks that are likely to be subjected to jamming, fading, and loss of resources.

Unit 17 is a cooperative research effort by Professors K. Arun, K. Jenkins, D. Jones, and V. Poor on adaptive signal processing, which seeks to develop new methods to extract and/or enhance time-varying (nonstationary) signals from additive noise. Both parametric and nonparametric approaches are investigated in this project for both narrow-band and wide-band signals of interest. The overall objectives are to develop computationally efficient adaptive time-frequency representations and new adaptation algorithms and filter structures that are computationally efficient for real-time applications, are robust, and are suitable for short wordlength VLSI implementation Professor V. Poor left the University in August 1990, and Professor T. Başar took over the supervision of his JSEP-supported doctoral students, who continue to work on the research of this JSEP research unit. Professor D. Jones and his research assistant R. Baraniuk obtained new results

in the development of a signal-dependent time-frequency analysis technique that is promising for the adaptive detection and classification of sonar transient signals. This result is cited in Section II as a JSEP significant accomplishment.

Director's Research Initiatives

Unit 18 provides the Director with discretionary funds to support early start-up on new projects that present immediate opportunities of high scientific promise, to provide matching funds for new equipment, and to help support promising work of new faculty whose interests are closely aligned with the JSEP program. During the first year of the current JSEP grant, four specific projects have received support from JSEP discretionary funds. These include support for special equipment needed to make low-temperature measurements on quantum devices fabricated under Unit 7, partial support for a JSEP supplementary project that could not be funded in the regular program (Professor C. Chuang, Unit 20), continuing support of the EpiCenter operating fund, matching equipment funds to help initiate a $450K state-funded applications research effort in acoustic charge transport (ACT) device technology, and summer support for several new faculty who are contributing to the current JSEP program. Details of these projects are reported in the main body of this report under Unit 18.

II. JSEP Significant Accomplishments (April 1, 1990 - March 31, 1991)

Two categories of "most significant accomplishments" are reported in this section and cited as important contributions that have been supported either in total or in part by the JSEP grant at the University of Illinois at Urbana-Champaign. In the first category, we cite three outstanding technical accomplishments that were direct results of JSEP research during the last year. Further details on these accomplishments are discussed in the main body of this report. In the second category, we cite recent extraordinary professional accomplishments of four individuals who have received JSEP support over the years through the Coordinated Science Laboratory and who have been indirectly nurtured in their accomplishments by JSEP support.

A. Recent Outstanding Technical Results

(1) Nano-Scale Engineering Using the Scanning Tunneling Microscope (Tucker and Lyding, Unit 5)

The thrust of the research by John Tucker and Joe Lyding under the JSEP Program centers on the use of the STM to probe small electronic device structures, with emphasis on III-V materials. They have recently completed a new UHV STM system, which includes basic sample preparation and characterization facilities (resistive and e-beam heating, Ar^+ sputtering, LEED, etc.). This permits a wide range of work on examining and designing semiconductor surfaces. In order to examine device structures, a fully integrated coarse translation system is being developed that allows the scan area of $10\mu m \times 10\mu m$ to be placed anywhere within a 2mm x 2mm area. A prototype is working on the bench, and the final design is near completion.

The combination of UHV STM with coarse translation will permit the probing of the properties of III-V heterolayers on a nanometer scale; such measurements will begin within the next few months. They will be able to cleave AlGaAs materials *in situ*, transfer them into the STM, and locate the heterolayer interfaces. STM spectroscopy can then be utilized to examine quantized energy states, level occupation, and band-bending as a function of external bias, all in a much more detailed manner than has previously been possible. If this works out as well as anticipated, it should be possible to make significant contributions toward understanding and optimizing many types of heterolayer devices.

In addition to its use as a diagnostic tool, the STM offers the potential for fabricating nanometer scale device structures through surface modification of various types. Using this JSEP research as a foundation, collaborations continue with Professor K. Hess to explore these possibilities, as well as to organize a proposal for the DoD URI programs on nanostructures and nanolithography.

Nano-Scale Gold Dots Written on a Gold Surface
with STM Techniques

(2) ILLIADS-R: A Fast Timing and Reliability Simulator (Kang and Shih, Unit 12)

One of the most difficult problems in handling increasing design complexity lies in the timing verification of the entire chip. Even with supercomputers, detailed circuit-level simulation cannot be adequately handled. As a result, for more than a decade the timing verification of digital VLSI chips has resorted to fast timing simulation packages. Conventional timing simulation programs had to use rather crude models of transistors or circuit primitives in order to reduce the computation time at a significant sacrifice of simulation accuracy. As a result, most existing timing simulators missed an entire cycle or more due to the accumulation of errors in multiple cycle simulation of VLSI circuits.

In order to address this serious problem in timing verification of digital MOS VLSI circuits, Kang and Shih have researched a new timing simulation approach that takes a drastically different formulation of the problem. Recently, they have successfully developed a new timing simulation program, ILLIADS (ILLInois Analogous Digital Simulator). ILLIADS contains over 30,000 lines of codes in C programming language, and it decreases the simulation time over SPICE-generation programs by a factor of 3N, where N is the number of transistors to be simulated. In other words, for a circuit containing, for example, 100,000 MOS transistors, ILLIADS can speed up the simulation time over SPICE or its derivative programs by 300,000 times with much better accuracy than any other timing simulation program. As far as they know, these achievements are superior to other timing simulators in both speed-up and simulation accuracy.

This drastic improvement has been made possible through the introduction of a new generic circuit primitive and a new rigorous analytical solution to nonlinear differential circuit equations, i.e., Riccati equations, under piecewise linear input waveforms. They have been able to simulate a digital MOS circuit containing 235,000 transistors in less than 10 minutes on a workstation with about 80 Mbytes of swapspace. Further research and development of ILLIADS should enable accurate simulation of digital MOS VLSI chips and even multichip modules (MCMs) with affordable computation time.

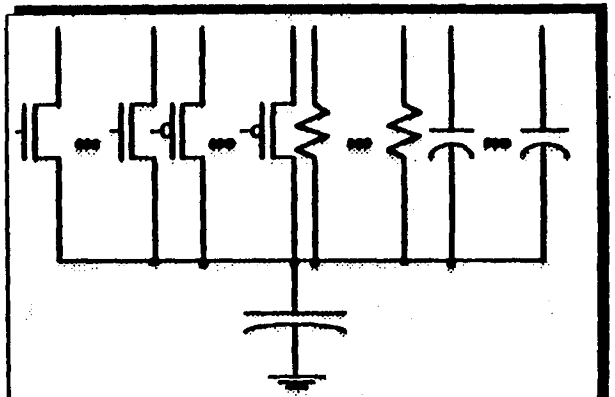
The current version of ILLIADS has already been used effectively in class projects (ECE 482, Physical Design of VLSI, spring 1991) and also for reliability simulation. For reliability simulation of hot-carrier-induced circuit performance degradations, they have implemented damaged MOS transistor models into ILLIADS-R, reliability simulator derived from ILLIADS, and have used ILLIADS-R to simulate and analyze long-term aging phenomena of MOS VLSI circuits with over 3700 transistors, which is another first-time achievement. The development of physical models and algorithms for reliability simulation has been funded by the Semiconductor Research Corporation (SRC) and the Rome Air Development Center. It was a very timely and almost perfect linkage between ILLIADS and the reliability simulation projects.

They also applied ILLIADS for mixed analog-digital circuit simulation. Since ILLIADS outputs analogous voltage waveforms, its interface with detailed circuit simulators like SPICE for analog simulation is natural and does not suffer from the signal mismatch problems faced by most mixed-mode simulators.

Thus, their research accomplishments are good examples of how JSEP research results of a high-risk project have impacted other research projects.

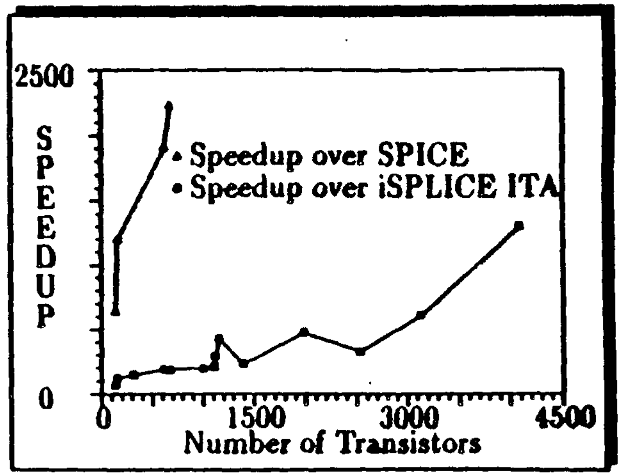
ILLIADS-R: A Fast Timing and Reliability Simulator

- Timing simulation is essential for VLSI design verification. Conventional timing analysis tools are not accurate enough nor can handle circuits as large as millions of transistors, especially at designer's workbench, i.e., workstation.
- ILLIADS-R solves timing simulation problems by introducing a new generic circuit primitive and solving Ricatti equations analytically.
- The speedup of ILLIADS-R vs. SPICE is ~3N, N is the number of transistors.
- A very large circuit consists of 235,000 transistors had been simulated on a DEC5000/200 workstation in 10 minutes real time with 80 Mbyes available swap space. With larger swap space, over one million transistors can be handled.
- ILLIADS-R has been applied to Hot-carrier damaged VLSI circuit simulation using 1-D damaged transistor model developed at U of I.
- ILLIADS-R is being technology transferred to industry and universities.



$$\frac{dV}{dt} = kV^2 + (p_1 t + p_0)V + (q_2 t^2 + q_1 t + q_0)$$

The Circuit Primitive



Speedup of ILLIADS-R

JSEP Highlight

(3) Signal-Dependent Time-Frequency Representations (Jones and Baraniuk, Unit 17)

Time-frequency distributions are used to analyze signals with time-varying frequency content in a wide variety of applications. Of particular interest to the defense community is the analysis of transient signals, both electromagnetic (e.g., in ELINT applications) and acoustic (as in SONAR applications). Time-frequency distributions are currently widely used in SONAR systems. The performance of detection and classification methods based on a time-frequency description of a signal clearly depends greatly on the quality of the time-frequency representation that is used. Current time-frequency representations, such as the short-time Fourier transform, the Wigner distribution, and the Choi-Williams distribution, apply a fixed smoothing kernel to suppress artifacts and noise. However, a fixed kernel severely limits the class of signals for which the representation performs well. The wide variety of signals encountered in the ocean acoustic environment, for example, prevents any fixed-kernel representation from delivering adequate performance.

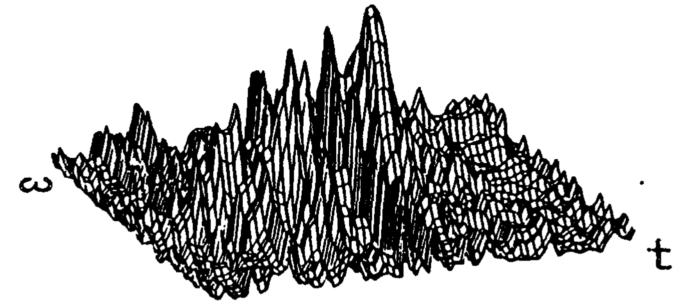
To overcome this fundamental difficulty, Jones and Baraniuk have developed a *signal-dependent* time-frequency representation, which, by automatically adapting the kernel to the data, can potentially achieve near-optimal performance for a much wider range of signals than any fixed-kernel method. The method designs an optimal signal-dependent kernel that suppresses noise and cross-term artifacts while minimizing auto-component distortion. The optimization requires solving a specialized linear program. They have developed an extremely efficient algorithm for computing the optimal kernel, with a computational cost comparable to standard fixed-kernel representations. The signal-dependent kernel design is surprisingly robust to additive noise, and performs well even at a 0 dB signal-to-noise level. The technique thus appears promising for adaptive detection and classification of acoustic transients.

The signal-dependent time-frequency representation appears very promising for analysis of SONAR transient signals, and a great deal of interest has been expressed by this community. Researchers at Hughes, ORINCON, and ESL have requested computer programs implementing this technique, and they will soon be evaluating the method for application in Naval SONAR systems.

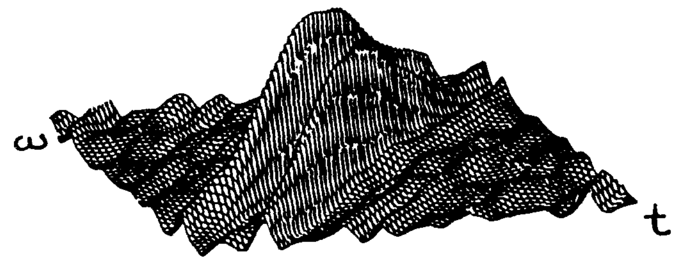
Signal-Dependent Time-Frequency Representations

- Time-frequency representations (TFRs) are powerful tools for analyzing signals with time-varying frequency content
- Defense applications:
    - transient SONAR signal analysis
    - RADAR signal processing
    - ELINT
- Any fixed TFR works well only for a limited class of signals
- A *signal-dependent* TFR overcomes this limitation
- An efficient, optimal design procedure has been developed

Wigner distribution



Choi-Williams distribution



Optimal signal-dependent TFR

B. Outstanding Professional Accomplishments of JSEP-Supported Faculty

We note with great pleasure that during the last year Professor J. Greene received the Swedish Erlanger Award for his contributions to thin film physics; Professor G. Stillman received the 1990 Gallium Arsenide Symposium Award and the Heinrich Welker Memorial Medal for his outstanding contributions to Gallium Arsenide device technology; and Professor P. Kokotovic was awarded the Georgio Quazza Medal of the International Federation of Automatic Control and named the Hendrik Bode Lecturer for the 1991 IEEE Decision and Control Conference for his outstanding contributions to the field of robust adaptive control. These three awards were mentioned in the previous text under the discussion of the units that currently support the work of these individuals.

In addition to these, Professor N. Holonyak was recently awarded the Presidential Medal of Science for his extraordinary contributions to the development of laser diodes and high-power semiconductor switching devices. Although Professor Holonyak does not currently participate in the JSEP program due to his many other commitments, his work was supported for many years by JSEP. It is a pleasure for the Department of Electrical and Computer Engineering and the Coordinated Science Laboratory to see the work of one of their most distinguished faculty receive the widespread recognition that it deserves.

WORK UNIT NUMBER 1

TITLE: Low-Energy Ion/Surface Interactions during Metal and Semiconductor Crystal Growth from the Vapor Phase: Control of Microstructure and Microchemistry on the Atomic Scale

SENIOR PRINCIPAL INVESTIGATOR:

J. E. Greene, Research Professor

SCIENTIFIC PERSONNEL AND TITLES:

D. Lubben, Postdoctoral Research Associate
F. Adibi, Research Assistant
L. Markert, Research Assistant
Y. W. Kim, Research Assistant

SCIENTIFIC OBJECTIVE:

The primary objective of this research program is to develop a detailed understanding of energetic particle/surface interactions for controllably altering nucleation and growth kinetics, microchemistry, and physical properties of metal and semiconductor films during deposition from the vapor phase by a variety of techniques including ion-assisted MBE, plasma-assisted CVD, sputter deposition, and *primary-ion deposition*. Low-energy ion/surface interactions allow the crystal grower additional dynamic control, at the atomic level, over microchemistry and microstructural evolution. Kinetic energy can be efficiently coupled to the growth surface thereby altering surface reactivity as well as adsorption, adatom diffusion, and nucleation kinetics. The ability to use such effects to advantage in "designing" new growth processes as well as new materials depends upon our understanding of the nature of ion/surface interactions, as well as thermal adatom/surface reactions, during deposition. This work is being pursued from both an analytical and an experimental point of view.

SUMMARY OF RESEARCH:

Surface Reactions, Elemental Incorporation Mechanisms, and Depth Distributions of Thermal and Accelerated Dopants During Si MBE

As device sizes continue to shrink, not only laterally but in depth, control of microchemistry at the atomic level becomes ever more important. One area in which this has immediate consequences is dopant incorporation in semiconductor films grown from the vapor phase. Incorporation may be limited not just by the initial sticking probability (i.e., the probability of chemisorption) but also by the combination of surface segregation and desorption. Surface segregation, in addition, results in dopant profile broadening. These problems are particularly acute in MBE Si where most of the common dopants used in bulk Si technology present problems when co-evaporated during film growth due to low incorporation probabilities (P, As, Sb, Ga, and In) and/or pronounced surface segregation (As, Sb, Al, Ga, and In).

Our approach for resolving the problems of low dopant incorporation probabilities and high segregation rates during Si MBE has been to employ accelerated-beam doping techniques using unique UHV-compatible, low-energy, high-brightness, ion sources developed under JSEP sponsorship. We have extended our pioneering work on In^+ ion doping (where we demonstrated increases in σ_{In} by more than six orders of magnitude and the first example of σ-doping during MBE

Si) to Sb^+. The kinetics of dopant incorporation were determined experimentally as a function of acceleration potential E_{Sb} = 0-200 V, T_s = 550-1050° C, and R = 0.2-3 μm h^{-1}. σ_{Sb} was up to 5 orders of magnitude higher than attainable using thermal beams. In fact, σ_{Sb} was unity for $E_{Sb} \geq 150$ V at $T_s \leq 850°$ C. At lower acceleration potentials, σ_{Sb} was dependent upon T_s and R (following behavior in agreement with the model described below). However, even at E_{Sb} = 25 V and $T_s \geq 650°$ C, σ_{Sb} was still more than an order of magnitude larger than for thermal doping. Moreover, surface-segregation-induced profile broadening Δ_{Sb}, which for thermal-beam doping was $\geq$ 80 nm/decade for $T_s \leq 650°$ C, was less than the SIMS depth resolution, $\approx$ 12 nm/decade.

We have recently demonstrated two-dimensional electron quantum-confinement in δ-doped MBE Si layers formed with low-energy Sb-ion doping. Previous results on δ-doping during MBE Si have required interrupted growth in order to trap the dopant and prevent severe surface segregation. That is, Si growth is stopped, the substrate is cooled to ambient temperature, a partial ML of dopant is deposited followed by a thin amorphous Si layer, and then the amorphous layer is crystallized by solid-phase epitaxy (SPE) at 700° C. However, this technique suffers from a number of drawbacks, not the least of which is the danger of contaminant adsorption at ambient temperature and dopant precipitation, defect formation, and dopant migration throughout the amorphous layer ($\geq$ 3 nm) during solid-phase epitaxy. In our case, we have fabricated the δ-doped layers with $N_{Sb}^{2-D} = 10^{12}$–$2x10^{14}$ cm^{-2} at growth temperature with the width of the dopant profile determined only by the straggle of the trapped ion distribution. We have observed quantum confinement in these layers using tunneling current measurements.

Secondary-ion mass spectrometry, capacitance-voltage measurements, and high-resolution cross-sectional transmission electron microscopy have been used to show that Sb δ-doped layers produced with $V_{Sb} \leq 200$ V were extremely sharp. Full width at half maximum (FWHM) intensities were $\leq$ 2 nm and no precipitation was observed for N_{Sb}^{2-D} values up to $1x10^{14}$ cm^{-2} (equivalent to $N_{Sb} = 1x10^{21}$ cm^{-3}). Observed FWHM values are in good agreement with calculations carried out using the multi-site dopant incorporation model discussed below, which show that the Sb ions are trapped in near-surface sites, with substitutional coordination, completely suppressing surface segregation.

The results for σ_{In} and σ_{Sb} as a function of E and T_s, at least for E < 200 eV, cannot be described simply as implantation since the projected ion range is of the order of lattice constants. Thus, we have extended our thermal-dopant incorporation model (discussed in previous reports) and developed a multi-site transition-state model, which explicitly accounts for surface reconstruction and dopant kinetic energy. In the case of MBE growth on Si(100)2x1, the model includes bond rotation and changes in backbond lengths (hence potential barriers) in the first 5 layers (surface, bulk, and three intermediate sites). Surface segregation, dopant desorption, incorporation, and bulk diffusion are included; and dopant depth distributions are obtained by solving simultaneous transition-rate equations for passage between adjacent sites. Site desorption and segregation potentials were obtained from our previous modulated beam mass spectrometry and thermally stimulated desorption experiments together with a new analytical technique that we have developed—concentration transient analysis (CTA). Model calculations were in good agreement with our experimental data for $\sigma(E_{Sb},T_s)$. However, we have recently found that the correct description of $\sigma_{Sb}(R)$ and $\Delta_{Sb}(R)$, as well as the prediction of the critical temperature for the transition between kinetically limited and equilibrium dopant surface segregation, requires the introduction of step flow and ledge capture kinetics into the model. We are presently combining the analytical results with molecular dynamics simulations discussed in a later section.

Electronic and Optical Properties of Accelerated-Ion Doped MBE Si

An essential question to be addressed in view of the excellent incorporation results obtained for accelerated-beam doping is whether low-energy ion bombardment results in residual lattice damage that degrades electrical and optical properties. Obviously, at sufficiently high acceleration energies and low growth temperatures, this will be the case. However, we showed last year that for Si films

grown at = 800° C, E_{In} = 200 eV or E_{Sb} = 150 eV, and R = 1-2 μm h^{-1}, all dopant atoms were incorporated into electronically active substitutional sites at concentrations at least up to $2x10^{18}$ cm^{-3} for In (exceeding the solid-solubility limit) and $2x10^{19}$ cm^{-3} for Sb. Temperature-dependent Hall measurements showed that carrier mobilities were equal to calculated theoretical limits (in fact, the In^+ doped films exhibited the highest mobilities ever reported for In-doped Si, film or bulk!).

We have more recently grown a series of 5–μm-thick As^+-doped films with concentrations between $2x10^{16}$ and $5x10^{17}$ cm^{-3} using E_{As} = 200-1000 eV at T_s = 500-800° C. σ_{As} was essentially unity in all cases (for thermal doping σ_{As} is unmeasurable, < 10^{-8}). The ion-doped films exhibited the first high-quality PL spectra ever reported for doped MBE Si. Sharp ($\leq$ 0.5 meV FWHM), very intense, no-phonon and TO and TA phonon-assisted bound exciton peaks were obtained. No peaks ascribable to residual ion-induced damage were observed in films grown at T_s = 800° C with E_{As} = $\leq$ 1000 eV or T_s = 650° C with E_{As} = 200 eV. In fact, these films exhibited two-phonon (TO + Γ) assisted bound exciton peaks, indicative of very high-quality material. DLTS measurements have shown no indication of deep traps in any of these films to within the resolution of the measurement ($\approx 10^{12}$ cm^{-3}). However, reducing T_s to 500° C with E_{As} = 200 eV gave rise to a strong ion damage PL peak at 1039.7 meV. Furthermore, both undoped and As^+ doped films grown at 500° C exhibited a gradual increase in PL background below 890 meV that we believe was due to quenched-in, growth-related point defects. DLTS measurements showed electron trap states ($\approx 10^{14}$ cm^{-3}) at energies of 0.06 and 0.52 eV below the conduction band edge. Clearly, at growth temperatures near and below 500° C, E_{As} will have to be decreased below 200 eV and we have now grown samples with E_{As} = 50 eV.

An even more stringent test of ion doping is B since B^+ ions have a larger projected range making defect annihilation during growth more difficult. As expected, minimum ion energies for obtaining defect free films had to be decreased compared to the As doping case. Nevertheless, sharp bound exciton peaks, including two-hole recombination and annihilation of multiexciton molecules consisting of up to four excitons, signaling extremely high-quality material, were obtained from films grown at T_s = 650° C with E_B and 800° C with E_b = 500 eV.

Molecular Dynamic Simulations of Low-Energy Ion/Surface Interactions during Si MBE: Accelerated-Ion Doping and Low-Temperature Epitaxy

We have developed a supercomputer code for carrying out molecular dynamics (MD) simulations, utilizing the Tersoff many-body potential, to investigate ion/surface interaction effects. The MD simulations are presently being used in conjunction with our analytical model of ion doping described above to understand the details of collisional lattice dynamics and ion-induced defect formation and annihilation. In addition, the simulations are providing, for the first time, insights into potential mechanisms for ion-irradiation-induced "low-temperature" epitaxy that has been reported by a number of groups for systems such as Ag/Si, Si/Si, and InAs/Si.

Our initial simulations were carried out for 10 eV Si atom bombardment of a Si lattice with a (001)2x1 reconstructed surface. The irradiation events were initiated at an array of points in the primitive surface unit cell. Each event was followed to determine kinetic energy redistribution in the lattice as a function of time, ion and lattice atom trajectories, and the nature, number, and depth of residual defects. Surface dimer breaking, epitaxial growth (due to both projectiles and lattice atoms coming to rest at epitaxial positions), and the formation of residual hexagonal and split interstitials composed of projectiles and/or lattice-atoms were observed. There were no residual vacancies. Impact points leading to each of the above results clustered in distinctly different regions of the surface unit cell.

Recently, we have used a combination of molecular dynamics and quasidynamics simulations to investigate the relaxation, diffusion, and annihilation of split and hexagonal interstitials resulting from 10 eV Si irradiation of (2x1)-terminated Si(001). Stable atomic configurations and total potential energies were derived as a function of site symmetry and layer depth. The interstitial Si atoms were

allowed to diffuse and total potential energy changes calculated. Lattice configurations along each path, as well as the starting configurations, were relaxed and minimum energy diffusion paths derived. The results showed that the minimum energy paths were toward the surface and generally involved tetrahedral sites. Calculated interstitial migration activation energies, even in the bulk, were always less than 1.4 eV and were much lower in the near-surface region than in the bulk. Thus, the defects could easily be annealed out over time periods corresponding to less than that required for monolayer deposition under typical MBE epitaxial film growth conditions.

The present calculations provide detailed insights concerning minimum energy diffusion paths in both bulk Si and near-surface regions, lattice relaxation around interstitial defects, bond breaking and reforming processes, and the nature of atomic configurations at saddle points in the potential energy surface for self-interstitial migration. Si self-interstitials created in the near-surface region (layer number < 6) exhibit much lower migration activation energies than bulk defects, due to more extensive relaxation of surrounding atoms, and diffuse preferentially through tetrahedral sites toward the surface. The role of the surface in exacerbating relaxation around shallow interstitials was stronger for defects located in regions between, rather than below, dimer rows leading to higher defect formation energies for the latter. We are presently extending these results to 50 eV in order to include vacancies and deeper layer effects.

Growth of High-Resistivity Wurtzite and Zincblende Structure Single Crystal GaN by Reactive-Ion Molecular Beam Epitaxy

Epitaxial GaN films have been grown at temperatures between 600 and 900° C by reactive-ion molecular-beam epitaxy. Ga was provided by evaporation from an effusion cell, while nitrogen was supplied from a low-energy single-grid ion source. The average energy per accelerated N incident at the growing film surface was ≈ 19 eV. Films deposited on Al2O3(0112) and MgO(001)1x1 substrates had wurtzite (α–GaN) and metastable zincblende (β–GaN) structures, respectively. The lattice constants were a = 0.3192 nm and c = 0.5196 nm for α–GaN and a = 0.4519 nm for β-GaN. The room-temperature optical bandgap E_g of zincblende GaN, 3.30 eV, was found to be 0.11 eV lower than that of the hexagonal polymorph α-GaN. All films were n-type with electron carrier concentrations, which decreased from 4×10^{18} to 8×10^{13} cm^{-3} with increasing incident N_2^+/Ga flux ratios between 0.63 and 3.9. Resistivities > 10^6 Ω–cm were achieved.

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WORK UNIT NUMBER 2

TITLE: A Merger of Monte Carlo Methods and Hydrodynamic Models in Computational Electronics

SENIOR INVESTIGATORS:

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U. Ravaioli, Research Assistant Professor

SCIENTIFIC PERSONNEL AND TITLES:

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SCIENTIFIC OBJECTIVE:

The development of physically accurate and computationally efficient device models continues to be of vital interest for the design and analysis of modern silicon VLSI circuits. In the past, we have developed very accurate Monte Carlo simulation tools. While these tools cover much of the important physics of fine line devices, they are computationally very intensive. We attempt, therefore, to merge the Monte Carlo methods with more standard approaches in two distinct ways. We believe that in this way we can achieve both physical accuracy and computational efficiency.

SUMMARY OF RESEARCH:

I. Augmented Drift-Diffusion Solver

We have implemented a robust program for the steady-state solution of semiconductor device equations based on an augmented drift-diffusion approach. Drift-diffusion (D-D) models still constitute the backbone of detailed device simulations, particularly in connection with device optimization and circuit simulation. As device dimensions have shrunk to submicron levels, the traditional current equation, with only the model of velocity saturation for the hot-electron effect, becomes inadequate, since velocity overshoot effects may be very important. An alternative way, the Monte-Carlo (MC) method, offers a rigorous description of semi-classical device physics but still requires very large computational resources and cannot be applied extensively to realistic device structures with high dopings. Thornber [27] has suggested a one-dimensional augmented D-D equation for modeling velocity overshoot effects. A number of simulation experiments in connection to this proposal have been performed for Si [28-32].

Our augmented D-D device simulator has been implemented in collaboration with Prof. Thomas Kerkhoven of the Computer Science Department. The simulator is called OSMOSIS (Overshoot Modeling Of Semiconductor Structures). The code uses the box integration method over a nonuniform rectangular grid.

In parallel white code development, we have pursued a theoretical investigation for a more rigorous formulation of the overshoot model. Two main theoretical results have been obtained: (a) an analytical formulation of the length coefficient $L(E)$ [33] which is the parameter containing the overshoot information, as a function of the local field E. An analytical form for

$L(E)$ is important both for comparison with particle Monte Carlo calculation and for a robust numerical implementation of the solution schemes; (b) a novel formulation of the two-dimensional augmented current equations [34]. This general equation has been obtained from an analysis of the energy balance equation and naturally deals with the problem related to the inclusion of confining fields, essential for the analysis of realistic devices.

In [34] it is also proven that the empirically derived form of the augmented cu-rent equation, relating the overshoot term to the space derivative of the quasi-Fermi level rather than the electric field [30], is a particular case of the new formulation. We are currently investigating the possible numerical implementation of this new 2-D augmented model. A challenging complication is due to the implicit dependence of the current density on itself, through the augmented term, which inevitably arises in a rigorous multidimensional formulation of the problem.

III. Hydrodynamic Semiconductor Equations

Our investigation of the "hydrodynamic" semiconductor equations has led to numerous new results, as well as extended collaborations and interdisciplinary interactions. The hydrodynamic model [35], consisting of the first three moments of the Boltzmann Transport Equation, is known to be incomplete in that an approximate closure relation must be invoked in order to make the system of equations soluble. This closure relation (in practice, a modified Wiedemann-Franz relation between the electrical and thermal conductivity serves this purpose) contains the information of all higher order moments that are not solved. Even for the relatively simple case of a 1-D $n^+/n/n^+$ silicon diode at room temperature, small changes in this approximate closure relation can cause the hydrodynamic model to converge to unphysical results. In collaboration with W. Fichtner (ETH, Zurich) and W. M. Coughran (AT&T Bell Laboratories), we have analyzed the limitation of the original hydrodynamic formulation and have investigated the use of Monte Carlo simulations to obtain accurate solutions for simple test devices, as well as to parameterize the transport coefficient.

The research activity has been expanded in the attempt to derive a model that corrects the problems of the hydrodynamic formulation. A novel energy balance equation approach has been formulated, extending the original approach by Stratton [36] in a rigorous way to the hot electron regime [37]. The new energy balance model avoids the evaluation of the moments of Boltzmann's equation and never invokes the Wiedemann-Franz law to model heat flow. Preliminary results on the 1-D $n^+/n/n^+$ silicon diode test structure shows a much better agreement with Monte Carlo results than the hydrodynamic model. An important feature of the new model is the reduced number of independent variables with respect to the hydrodynamic model, which is of paramount importance for an extension to multidimensional simulations.

The results of our activity have generated several new collaborations. An ongoing interaction with Prof. Robert W. Dutton of Stanford University aims at the inclusion of the new energy balance model as a "window" option inside a specified domain of semiconductor devices studied with the standard drift-diffusion simulator PISCES. A novel 2-D discretization approach has been proposed for the energy balance equations [37]. In addition, an effort is under way to calculate the transport parameters in the energy balance model using a Monte Carlo approach for Si and GaAs.

A collaboration has also been initiated with a group of applied mathematicians (Prof. Joseph Jerome of Northwestern University and Prof. Chi-Wang Shu of Brown University) to compare different formulations of hydrodynamic-like models and to study efficient solution methods, based on time-dependent iterations, that are amenable for a simple and efficient extension to 2-D and 3-D. Methods that can be naturally implemented on vector and parallel supercomputers are particularly emphasized.

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WORK UNIT NUMBER 3

TITLE: Gas Source Molecular Beam Epitaxy/Chemical Beam Epitaxy for Optoelectronic Devices

SENIOR INVESTIGATORS:

G. E. Stillman, Research Professor
K. Y. Cheng, Research Associate Professor

SCIENTIFIC PERSONNEL AND TITLES:

E. J. Roan, Research Assistant
A. P. Curtis, Research Assistant

SCIENTIFIC OBJECTIVE:

The objective of this research unit is to develop the gas source molecular beam epitaxy (GSMBE)/chemical beam epitaxy (CBE) technique for the growth of high-speed and high-efficiency optoelectronic device structures based on phosphorous-containing III-V compound semiconductor heterojunctions. The epitaxy system and the growth process will be developed and optimized to yield improvements in the epitaxial layer purity, interface quality, reproducibility and uniformity of composition, thickness and doping, and a reduction of the surface defect concentration. Heterojunction and/or superlattice structure devices including heterojunction bipolar transistors, avalanche photodiodes, and quantum well lasers will be prepared and investigated.

SUMMARY OF RESEARCH:

A considerable amount of progress has been made in the area of GSMBE technology development. Last year, a comprehensive analysis of the column V (As and P) memory effect has been performed resulting in a redesign and reconstruction of the hydride gas crackers/injectors and the gas handling system.

The optimum gas injector structure should produce a maximum dimer flux from the hydride source, but at the same time not totally compromise the ability to turn it off. A fully open injector design would produce optimum switching, but it would require the use of high injector temperatures to produce substantial dimers. A heavily baffled design would limit the pumping speed through the injector, while not necessarily guaranteeing an all dimer column V source. The injector design was chosen to be somewhere between the two extremes. Figure 1 shows the resulting injector. It consists of a 0.5 in.-diameter Ta tube, 7.5 in. long, inserted into a 7.5 in.-long Mo tube, which was itself connected to a 4.5 in. water-cooled flange where the gases are injected. Mo was chosen because it has almost no catalytic effect on AsH_3 and PH_3. Approximately one inch inside the Ta tube was inserted a Ta cone supported by a Ta rod giving it a "dartlike" structure. The Ta dart is used to act as a gas deflector to force virtually all the gas to come into contact with hot Ta, where it can be catalyzed. The Ta section is heated by a pyrolytic boron nitride/pyrolytic graphite tube, which is itself surrounded by a Ta heat shield. The flow controllers used for both AsH_3 and PH_3 were MKS type 1259B. The pressure at the inlet side to the injector, estimated from the line pressure, is ~100 Torr. The gas cracking and switching characteristics for this new injector and gas handling system were determined by in-situ time-resolved quadrupole mass spectroscopy (QMS). The column V memory effect has been virtually eliminated with a switching time on the order of 60 ms.

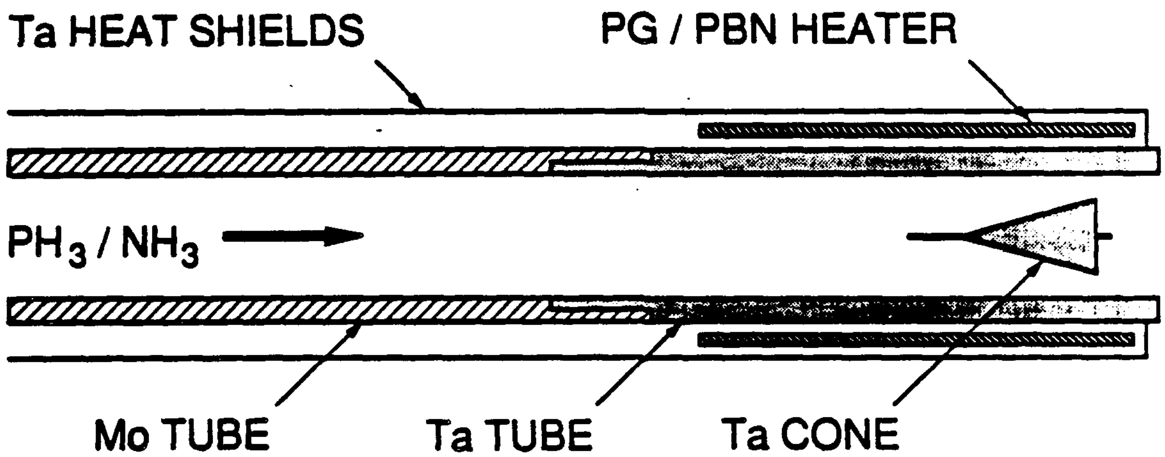

Fig. 1. Schematic drawing of the PH_3 and AsH_3 high pressure gas cracker/injector.

A comparison of various gas cracking catalysts (Ta and W) has also been performed in an effort to optimize the gas switching performance while maintaining the superb dimer/tetramer ratio that had been obtained with the previous heavily-baffled gas cracker design. It was found that the Ta gas cracker provides not only a higher peak As dimer/tetramer ratio, but also that this peak ratio occurs at approximately 100°C lower cracker temperature than for the W gas cracker. The Ta gas cracker has a cracking efficiency higher than 99% at temperatures as low as ~750°C for both AsH_3 and PH_3. An uncorrected dimer to tetramer ratio of >45 for P has been obtained. This work has resulted in an optimized hydride gas cracking injector that has both fast switching and predominantly dimeric beam flux. High quality AlGaInAsP epitaxial layers with accurate control of As/P ratio and abrupt As/P interfaces are expected to be grown in the near future.

Layers of InP with low residual carrier concentrations (~$1 \times 10^{15} cm^{-3}$) and reasonably high electron mobilities (~60,000 cm^2/v–s) as well as narrow double crystal x-ray diffraction (DCXD) peaks (Full-Width-at-Half-Maximum ~ 11.5 arcsec) have been grown by GSMBE. Lattice-matched layers of $In_{0.53}Ga_{0.47}As$ have been grown on InP substrates, and the growth conditions are currently being optimized as determined by DCXD, low temperature photoluminescence, and Hall measurements. Doping studies are also being conducted in InP and $In_{0.53}Ga_{0.47}As$ in order to optimize the material characteristics for heterojunction photonic and electronic device applications. This includes contact resistance studies for the Si-doped $In_{0.53}Ga_{0.47}As$ contact layer for the heterojunction bipolar transistors (HBTs) and laser diodes, as well as determining the optimal growth conditions for the heavily Be-doped $In_{0.53}Ga_{0.47}As$ base region of HBTs. The interface abruptness of $InP/In_{0.53}Ga_{0.47}As$ heterostructures has been studied using secondary ion mass spectroscopy (SIMS). The SIMS data indicate that the As/P memory effect has been totally eliminated.

To further enhance the optical efficiency in GaP grown by GSMBE, the generation and incorporation of isoelectronic nitrogen centers have been investigated. The thermal dissociation of the nitrogen source, NH_3, injected through a Ta-based high pressure (~100 Torr) gas injection cell was studied using the QMS technique. At ~ 700°C, Ta was found to effectively dissociate the NH_3 into primarily N_2 and H_2 molecules. However, the number of N atoms incorporated was too low to

generate efficient luminescence. When NH_3 and another hydride were coinjected, more than $2x10^{20}cm^{-3}$N atoms can be substitutionally incorporated into the GaP epitaxial layer. As shown in Figure 2, the 77 K photoluminescence spectra of a sample with a N concentration of ~$5x10^{19}cm^{-3}$ indicated the dominant emission wavelength was at 5691 Å (2.18 eV), which is characteristic of the nearest neighbor pair transition NN_1. The corresponding yellow-green photoemission is consistent with that observed for N-doped GaP grown by liquid phase epitaxy (LPE). The maximum N concentration was found to exceed that which can be produced through either LPE and VPE processes. Significantly higher N concentrations are believed possible with this growth technique.

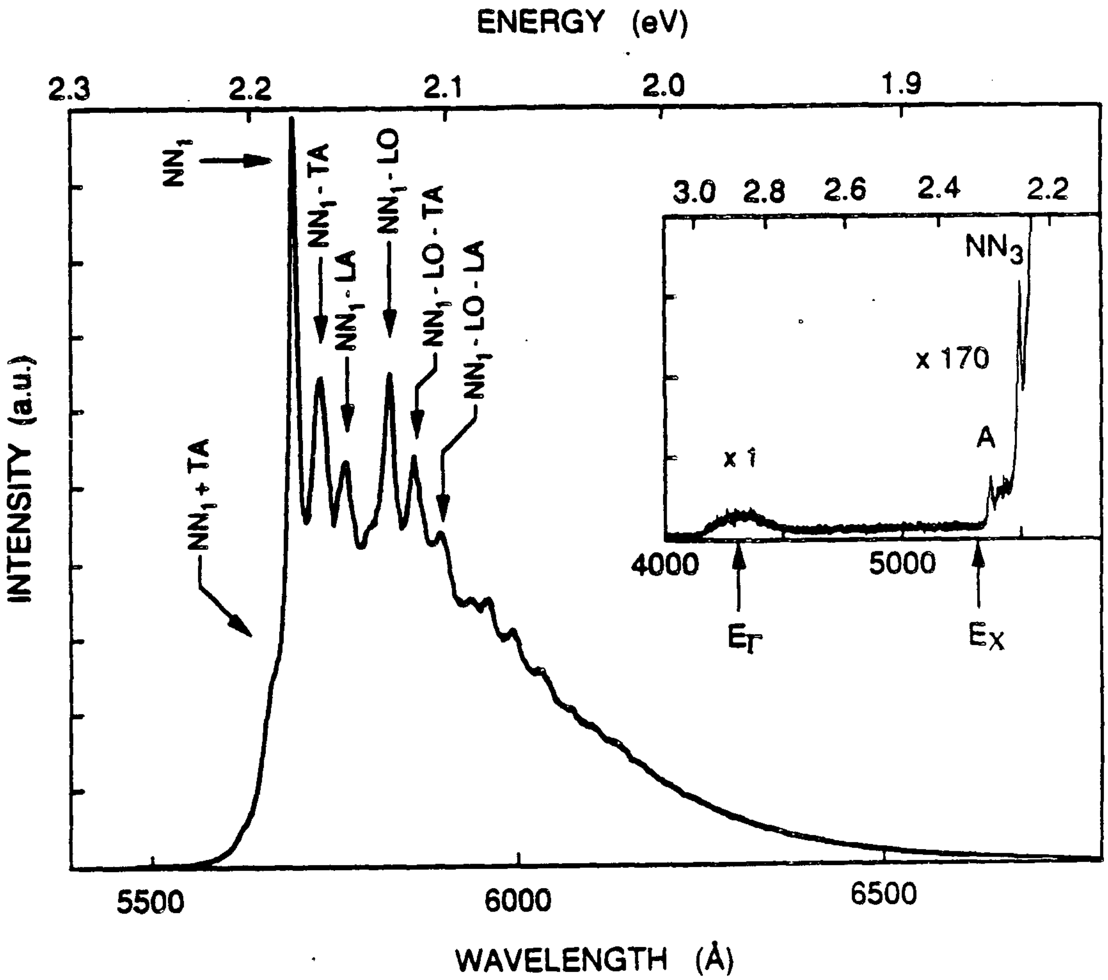

Fig. 2. The 77K photoluminescence spectra for a GaP sample with 4 – 5 x 10^{19} cm^{-3} nitrogen. The incident UV power density is 150 mW/cm^2, and the entrance and exit slits are 50μm. The dominant emission line at 5691 Å is the NN_1 pair transition. The higher energy transitions are from the NN_3 pair, A-center, and direct energy gap (insert). The local mode can be detected on the higher energy shoulder of the NN_1–LO transition.

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WORK UNIT NUMBER 4

TITLE: Heterostructure Electronic and Optoelectronic Devices by Metalorganic Chemical Vapor Deposition (MOCVD)

SENIOR INVESTIGATOR:

J. J. Coleman, Research Professor

SCIENTIFIC PERSONNEL AND TITLES:

M. E. Favaro, Research Assistant

SCIENTIFIC OBJECTIVE:

The objective of this program is to extend to electronic and optoelectronic integrated devices the enormous impact that metalorganic chemical vapor deposition (MOCVD), as a sophisticated epitaxial growth method, has had on optical device research. This involves fundamental studies of the electronic properties of heterostructure electronic materials, studies of devices made from these materials, and extension of these studies to integrated optical and electronic devices. Two specific areas of interest for this research are: (1) continued development of MOCVD-grown real-space transferred electron devices, the heterostructure hot electron diode (HHED), and other electronic devices, and (2) development of multi-terminal integrated laser structures, in which monolithic drive or modulation electronic devices are incorporated.

SUMMARY OF RESEARCH:

Negative differential resistance due to real-space transfer is observed when electrons, heated by the application of an electric field parallel to the GaAs-AlGaAs heterostructure layers, are thermionically emitted from a higher mobility layer (typically GaAs) into a lower mobility layer (typically AlGaAs). Two novel three-terminal devices utilizing the real-space transfer effect are the negative resistance field-effect transistor (NERFET) and the charge-injection transistor (CHINT). Both devices consist of a channel with two contacts (source and drain) and a conducting substrate, separated by a semi-insulating barrier. By applying a sufficient source-to-drain voltage, electrons are heated by the electric field and thermionically emitted over the barrier into the substrate. This produces an increase in the substrate current, which is the basis for the charge-injection transistor, and a decrease in the drain current with the associated negative differential resistance in the drain circuit, which is the basis for the negative resistance field-effect transistor. In the past year, we have continued our work on these real-space transfer devices. The structure of interest, grown by metalorganic chemical vapor deposition (MOCVD), consists of a n-type GaAs conducting layer, a 2000 Å $Al_{0.45}Ga_{0.55}As$ nearly insulating barrier layer, a lattice-mismatched (~150 Å) strained $In_xGa_{1-x}As$ electron channel layer, and a 1850 Å nominally doped GaAs cap layer. For sufficiently thin strained-layers, the strain is accommodated elastically and the layer remains commensurate with the substrate. At room temperature, an average drain current peak-to-valley ratio of 1.7 is measured for devices without an $In_xGa_{1-x}As$ channel. As the percentage of indium in the channel is increased, the drain current peak-to-valley ratio is observed to increase. At a channel indium mole fraction of $x = 0.22$, an average drain current peak-to-valley ratio of over 700 is measured at room temperature. The highest peak-to-valley ratio measured was 1270.

A critical step in the fabrication of the NERFET/CHINT devices is provision for shallow ohmic contact to the electron channel. In our present devices AuGe/Ag/Au contacts are carefully alloyed to avoid penetration into the $Al_{0.45}Ga_{0.55}As$ insulating barrier. In an effort to improve the reproducibility of contact formation, we have begun investigating Ge/Pd nonalloyed ohmic contacts. These Ge/Pd contacts are sintered at 350-375°C for 30 minutes in a hydrogen atmosphere. It has been shown that these contacts consume approximately 40 Å of GaAs and have a penetration depth of less than 100 Å. Our initial device structure consists of an n-type GaAs conducting layer, a 2000 Å $Al_{0.45}Ga_{0.55}As$ potential barrier, a 150 Å lattice-mismatched $In_{0.22}Ga_{0.78}As$ electron channel, a 400 Å lightly doped (n-type, $1x10^{16}cm^{-3}$) GaAs layer, and a 200 Å heavily doped GaAs cap layer (n-type, $1x10^{18}cm^{-3}$). Room temperature negative differential resistance was observed but with smaller currents and peak-to-valley ratios than the AuGe/Ag/Au ohmic contact system.

Since in the charge-injection transistor, the substrate or injection current at a given substrate bias is controlled by the drain voltage, we have attempted to use this current to modulate a laser diode. The integrated device structure consisted of a NERFET/CHINT device grown monolithically above a separate confinement heterostructure quantum-well laser. The laser structure consists of a 0.25 μm thick GaAs:p^+ buffer layer grown on a (100) GaAs:p^+ substrate, 1.5 μm thick p- and n-type $Al_{0.40}Ga_{0.60}As$ confining layers, a 50 Å GaAs quantum well centered in a 2000 Å $Al_{0.20}Ga_{0.80}As$ carrier collection region, upon which the NERFET/CHINT structure was grown. The NERFET/CHINT structure consists of a 0.5 μm GaAs:n^+ collector layer, a 2000 Å $Al_{0.45}Ga_{0.55}As$ barrier, a 150 Å lattice-mismatched strained-layer $In_{0.20}Ga_{0.80}As$ electron channel, and a 1850 Å nominally undoped GaAs cap layer. A photomask set was designed and fabricated that allowed the characterization of the NERFET/CHINT and the laser separately. Negative differential resistance and charge-injection into the substrate has not yet been observed.

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WORK UNIT NUMBER 5

TITLE: Scanning Tunneling Microscopy of Semiconductor Devices

SENIOR INVESTIGATORS:

J. R. Tucker, Research Professor
J. W. Lyding, Research Associate Professor

SCIENTIFIC PERSONNEL AND TITLES:

T. C. Shen, Postdoctoral Research Associate

SCIENTIFIC OBJECTIVE:

The scanning tunneling microscope (STM) makes it possible to probe electronic device structures on the atomic scale. The novel STM design developed by one of us (JWL) possesses several unique features that enhance its capabilities for such applications: (1) it is a true temperature-variable instrument capable of operating from liquid-He temperatures up to about 420K; (2) it requires little or no vibration isolation and is thus very compact; and (3) the measured thermal drift of <1Å/hour is nearly undetectable. This new STM design is currently marketed by three companies under license, including a low-temperature model and an ultra-high vacuum (UHV) version.

The primary goal of our research is to utilize this new STM to characterize, and to eventually modify, small electronic devices. In particular, we intend to focus on: (1) atomic resolution imaging and spectroscopy of AlGaAs heterolayers and interfaces; (2) studies of hot electron effects in the presence of strong electric fields; and (3) use of the STM as a tool for producing nanometer scale surface modifications, with an eventual goal of achieving a practical STM nanolithography.

SUMMARY OF RESEARCH:

During the past year, we have completed construction on the first chamber of our new UHV-STM system illustrated in Figure 1a. This chamber contains load-locking and sample cleaving capabilities together with several of the standard surface science tools, including sample heating, Ar+ sputtering, LEED, gas dosing arrays, in addition to the STM itself. Excellent atomic resolution images of the Si (111) 7x7 reconstruction have been repeatably obtained, as shown in Figure 1b, along with atomic resolution images of cleaved GaAs (110) surfaces.

A unique coarse translation system has also been implemented within our STM design during the past year. This modification allows us to translate the $10\mu m$x$10\mu m$ scan of the STM anywhere within a region of roughly 3mmx3mm, making it possible to locate particular features and device structures within this area. Thus far, we have used this technique to locate the boundaries of the depletion layer in Si p-n junctions and, also, to image the gate region of Si MOSFET structures as shown in Figure 2. These Si MOSFET structures have been specially fabricated for the purpose of STM alteration by Ted Higman at the University of Minnesota, as part of a collaboration with ourselves and Karl Hess. The goal here is to explore the possibilities for STM-induced surface modification within the gate region that could lead to new device characteristics. The Si p-n junction and MOSFET gate surfaces explored thus far have been passivated and imaged in air. The coarse translation system is currently being installed onto our UHV-STM, and this should allow us to begin probing the electronic properties of AlGaAs heterolayer structures on the nanometer scale, as well as examining Si p-n junctions in a controlled environment.

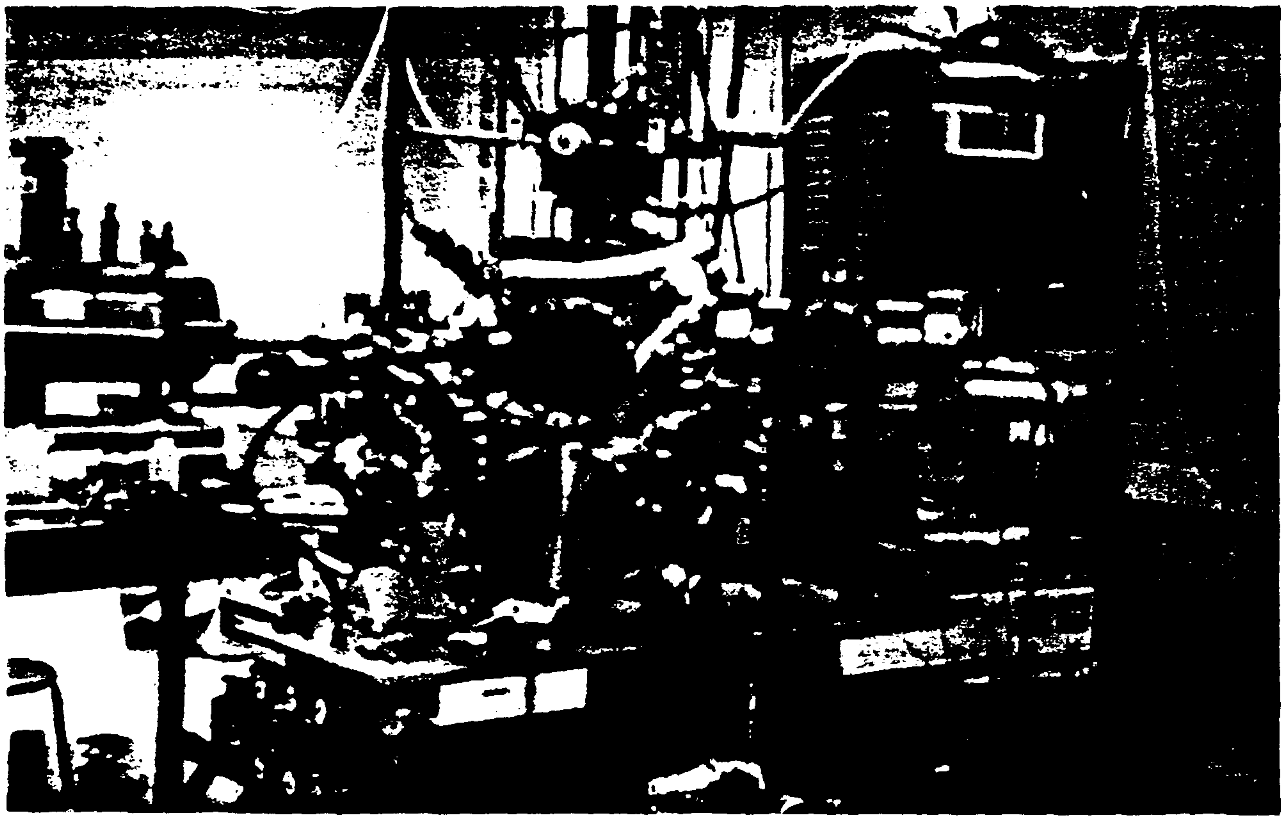

Fig. 1a: Photograph of new UHV-STM system.

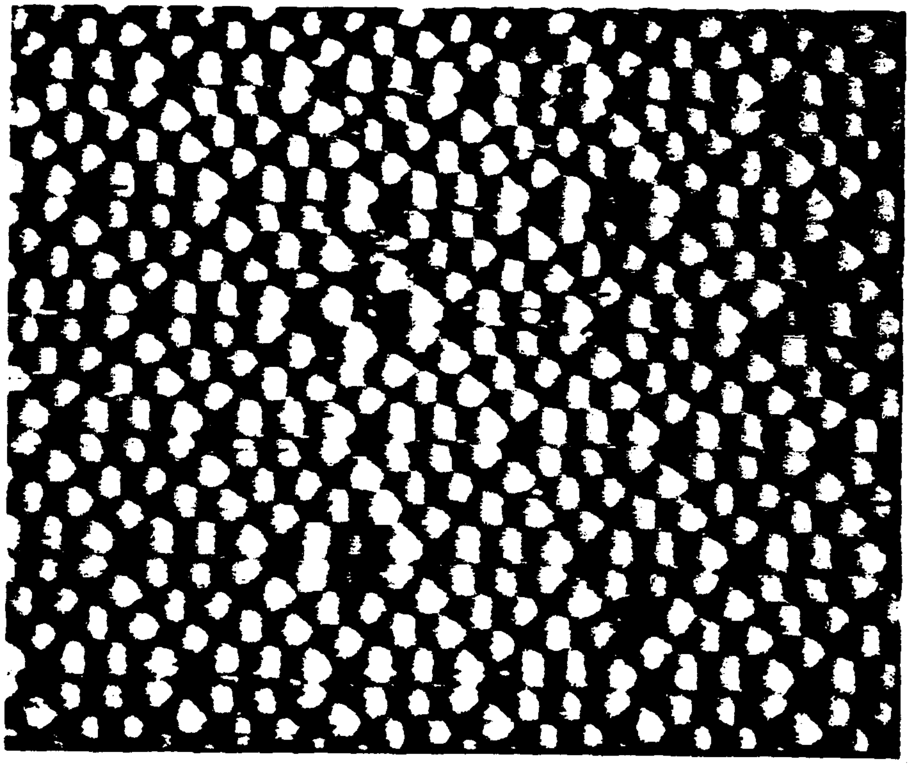

Fig. 1b: STM image of Si(100) 7x7 reconstruction at a sample bias of -1.5 V.

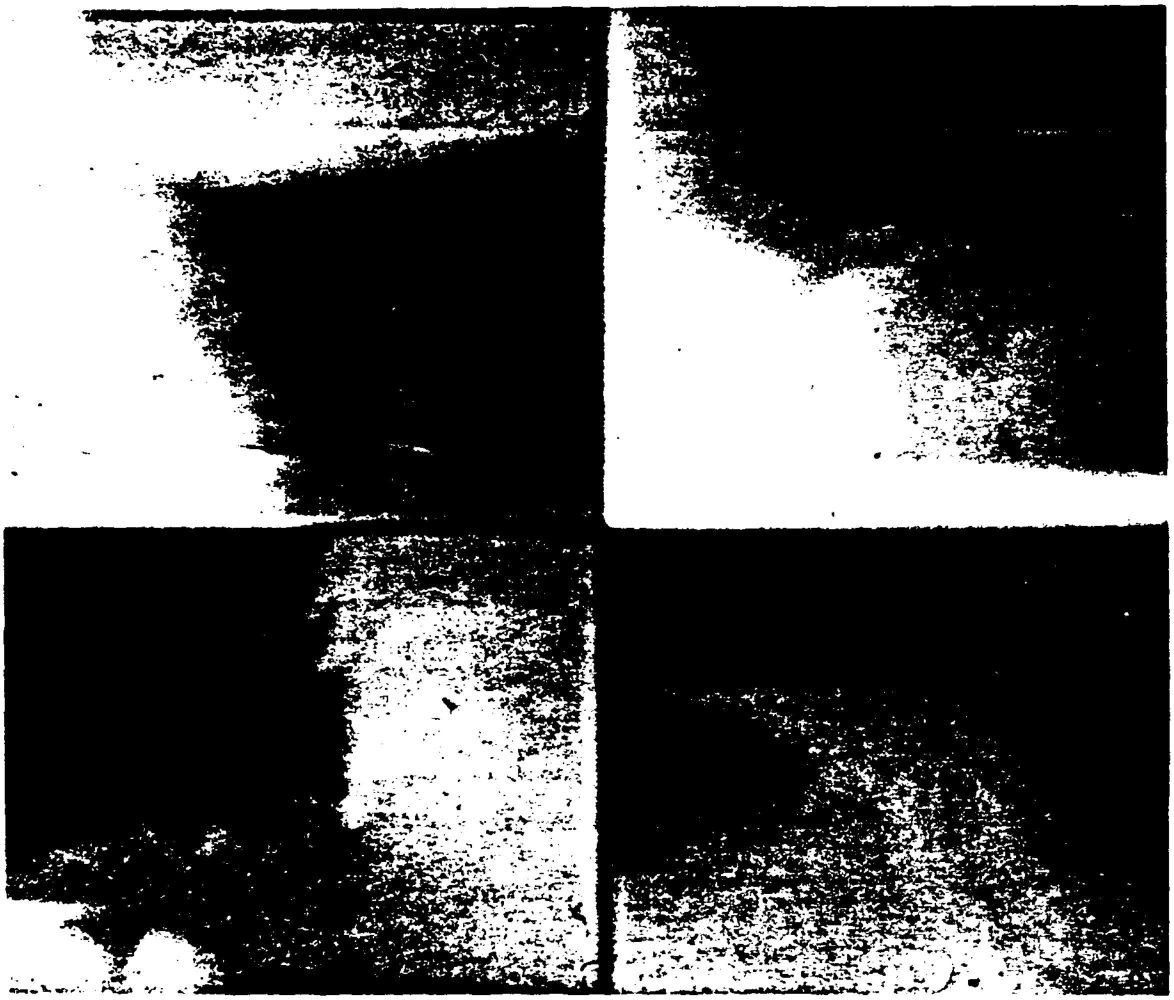

Fig. 2: STM images of a Si MOSFET structure located with the new lateral translation capability. Three of the images show corners of a source/drain depression while the fourth image (lower right) shows the gate region. Images are 8 μm x 8 μm.

Some preliminary experiments have been carried out already on surface modification and lithography. Holes as small as ~15Å have been created in graphite by means of current pulses applied to the STM tip, and dots of approximately 125Å in diameter and 30Å in height have been deposited by field evaporation from a Au tip onto a Au substrate, reproducing results first achieved at IBM. We expect that work on STM nanolithography will expand substantially during the coming year. Construction is now under way on a second UHV chamber that allows the STM port to be gated off with separate pump lines. This system will be utilized for experiments on STM-induced etching and deposition, involving reactive gasses that should not be introduced into our main surface science chamber.

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WORK UNIT NUMBER 6

TITLE: Reproducible Semiconductor Laser Frequency Standard: Devices Based on Rare Earth Ions in III-V Materials

SENIOR INVESTIGATORS:

J. G. Eden, Research Professor
M. J. Kushner, Research Associate Professor
J. T. Verdeyen, Research Professor

SCIENTIFIC PERSONNEL AND TITLES:

R. Fraser, Research Assistant

SCIENTIFIC OBJECTIVE:

To probe by femtosecond laser pump-probe techniques the processes by which excitation transfer occurs between Er^{3+} and a III-V semiconductor host.

SUMMARY OF RESEARCH:

I. Introduction

For over a decade, it has been known that excitation transfer from a III-V semiconductor host, such as GaAs or InP, to a trivalent rare earth ion occurs quite readily. That is, if GaAs, for example, is doped with one of the rare earth ions, the production of e-h pairs in the semiconductor results in the characteristic fluorescence lines of the atomic ion. Despite a number of excellent studies conducted primarily in the early 1980s, the mechanisms by which this excitation transfer takes place are still not understood. Several possible mechanisms have been proposed, but distinguishing among them requires that temporally resolved measurements be made on the subpicosecond time scale.

The implications of III-V → rare earth excitation transfer for optoelectronic devices are potentially quite significant. NTT Laboratories in Japan has successfully grown device-quality Er:GaAs layers by MOCVD that are suitable for ultimate use as master oscillators in an optical communications system. While activity in this country has been comparatively small, identification of the key mechanism by which excitation transfer takes place will undoubtedly suggest avenues for improving the process and constructing useful devices. The narrow emission linewidths of the rare earths in virtually any crystalline host make them especially attractive for use as an integrable and reproducible frequency standard.

For these reasons, we have been pursuing femtosecond laser pump-probe techniques as a means of unraveling the physics of the excitation transfer process. The next section describes the progress made thus far.

II. Progress To Date

A. Femtosecond System

Several major milestones have been reached, particularly in the last six months, toward completing these experiments. The femtosecond system and its associated diagnostics have been fully operational since last fall. The oscillator is a colliding pulse mode-locked (CPM) laser producing ~50 fs FWHM pulses at a PRF of 82 MHz. The energy of pulses directly from the oscillator is too low to be useful, in general, so a four-stage amplifier (operating at 10 Hz) increases the pulse energy to ~1/3 mJ. Dispersion in the amplifier chain increases the pulsewidth to ~300 fs and so a three-prism compressor was installed to re-compress the pulses to 50-60 fs FWHM. Figure 1 shows an autocorrelated pulse that is typical of those obtained from this system. The solid curve in the figure is the $sech^2$ best fit to the autocorrelator data.

Once the 1/3 mJ, ~50 fs pulses are generated, each pulse is split into two components. One component is time-delayed by a retro-reflector mounted on a computer-controlled micropositioner and is focused into one of several liquids to generate a supercontinuum. Figure 2 shows the continuum produced by irradiating butyl acetate.

Consequently, the experimental approach is straightforward. The first (red) pulse produces e-h pairs in the semiconductor host and the time-delayed probe interrogates the excited states of the rare earth ion.

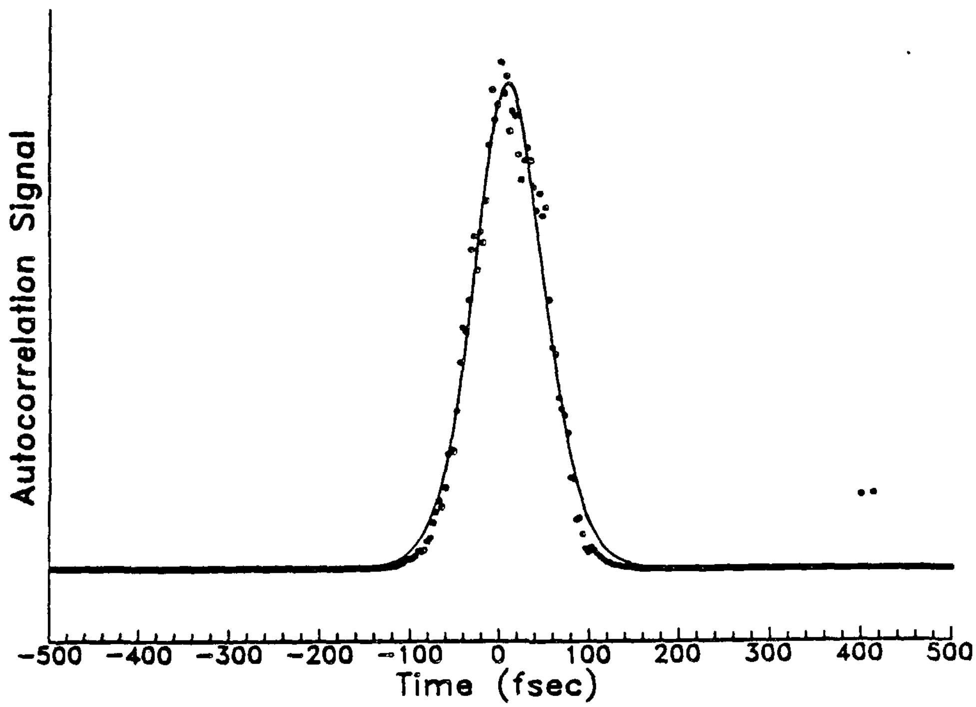

Fig. 1. Autocorrelation trace of a 59 fs FWHM pulse. The solid curve is the best fit of a $sech^2$ function to the data.

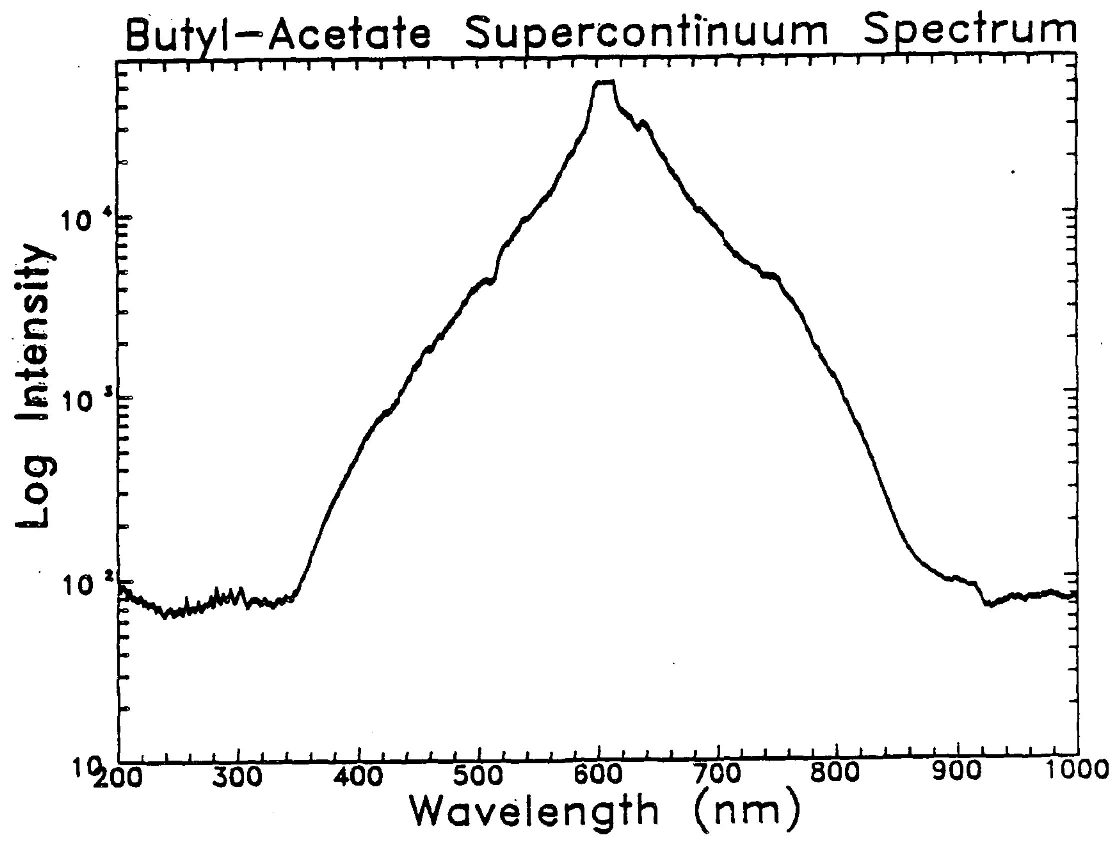

Fig. 2. Spectrum of the supercontinuum produced by focusing ~1/3 mJ, 50 fs pulses ($\gamma \approx$ 620nm) into butyl acetate.

B. Samples

Obtaining samples has proven to be a time-consuming process. Dr. Pomrenke of AFOSR has graciously provided several implanted samples and, after a considerable search, we have also located a source for MBE grown samples. Dr. Keith Evans of the Electro-Optics Technology (ELOT) Group at WPAFB has given us several Er:GaAs and Er:AlGaAs samples grown on GaAs. The Er-doped layers are 2 μm thick and the Er concentration varies from $\sim 10^{18}$ to $10^{19} cm^{-3}$. Photoluminescence experiments show clearly that the film quality depends strongly on the growth temperature and Er^{3+} number density, but emission at 1.54 μm from the Er^{3+} $^4I_{13/2} \rightarrow {}^4I_{15/2}$ transition of the ion has been observed for properly grown samples. Recent x-ray diffraction measurements on an MBE grown Er:AlGaAs shows the crystalline quality of the sample to be excellent despite an Er number density of $\sim 5 \cdot 10^{18}$ cm^{-3}.

C. Experimental Results

The pump-probe absorption measurements have not yet been completed, but two significant results have been reached. The first is that strong band-band emission has been observed from the doped GaAs layers when they are pumped by the femtosecond pulse. An infrared-to-visible fluorescence converter is now being installed on our photomultiplier to detect the IR lines of Er^{3+}, but these results demonstrate that signals of more than adequate S/N ratio are produced in this experiment. This is a result of a fiber optics bundle/lens telescope fluorescence collection system that was developed for these experiments.

The second obstacle that has been removed is the separation of Er-doped epilayers from the GaAs substrate in the MBE samples. Carrying out pump-probe absorption measurements on these samples requires that we probe only the epi-Er:GaAs or AlGaAs layer itself. The underlying substrate is thick compared to the doped layers and severely attenuates the probe (continuum) beam. Working with Prof. Jim Coleman, a graduate student has successfully removed the GaAs substrate from an AlGaAs overlayer. The WPAFB Er:$Ga_{1-x}Al_xAs$ layers have x ~0.5 that has a bandgap in the red. Removing the substrate gives us more spectral "room," and we expect soon to have the absorption spectra for both the Er:GaAs and Er:GaAlAs samples.

In summary, the work of the last six to eight months, in particular, has been fruitful and several experimental hurdles, including sample acquisition and preparation and signal detection, have been overcome. Over the next few months, we expect to observe the host → ion excitation transfer process in Er:GaAs and Er:GaAlAs in real time.

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WORK UNIT NUMBER 7

TITLE: Electronic and Transport Properties of Ultra-Low-Dimensional Semiconductor Structures

SENIOR INVESTIGATORS:

I. Adesida, Research Assistant Professor
J. P. Leburton, Research Associate Professor

SCIENTIFIC PERSONNEL AND TITLES:

D. Jovanovic, Research Assistant
K. Nummila, Research Assistant

SCIENTIFIC OBJECTIVE:

This work unit explores the potential of ultra-low-dimensional semiconductor structures for electronic and optical device applications. The emphasis is placed on fast transients and the research is concerned with the conception, design, and investigation of nonconventional devices characterized by extreme quantization of the electronic system.

Our method involves an integrated theoretical and experimental approach including various technological components from material growth, processing, and testing to numerical simulation of nanostructures. In addition, we are conducting a fundamental investigation of new physical effects in ultra-low-dimensional systems.

SUMMARY OF RESEARCH:

I. Materials and Fabrication

(a) Materials

With the departure of Professor J. Kolodzey from the University of Illinois, we have obtained MBE materials from Northeast Semiconductors Inc. and from Professor K. Y. Cheng of the University of Illinois. These materials include MESFET, conventionally doped and δ-doped MODFET layers. GaAs/AlGaAs MODFET layers with mobility in excess of 120,000 $cm^2-V^{-1}s^{-1}$ at 77 K have been obtained for the fabrication of one-dimensional devices. An inverted δ-doped MODFET heterostructure using an undoped AlGaAs as the Schottky contact layer is being evaluated for high mobilities and high carrier concentrations using Hall effect measurements. The thin AlGaAs layer will also permit the placement of the Schottky contact very close to the channel resulting in effective charge modulation. Heterostructures with pseudomorphic InGaAs channels will also be investigated.

(b) Nanofabrication

The effects of selective reactive ion etching (SRIE) in $SiCl_4/SiF_4$ plasmas on modulation-doped GaAs/AlGaAs heterostructures have been investigated using Hall effect measurements. It was found that extended etching and/or etching at high plasma self-bias voltages degraded the two-dimensional electron gas carrier concentration and mobility. The degradation is sufficiently minimized for low plasma self-bias voltages (< 30 V) and short etch times such that the SRIE process should be useful

for fabricating MODFETs. We have developed nanolithography on a scanning electron microscope capable of delineating 25 nm isolated metal lines and 60 nm T-shaped metal structures. These processes are being used to fabricate various devices for investigations of quantum effects. One of the principal investigators (I.A.) obtained an Illinois State Challenge Grant in December 1990. This grant is being used to upgrade the Cambridge electron beam lithography system, purchase a new electron beam evaporator and a sputtering system, and refurbish the chemically assisted ion beam etching (CAIBE) equipment. All these efforts will be accomplished during the summer of 1991, and they will significantly enhance our nanofabrication capabilities.

(c) Device Fabrication

We have fabricated GaAs MESFETs with gates as small as 30 nm. The MESFET layer was grown by MBE on semi-insulating GaAs and consists of a 1μm buffer layer, 25 nm n+ GaAs (4 x 10^{18}cm^{-3}), 2 nm AlAs etch stop layer, and 25 nm n+ GaAs cap layer. The etch stop assured identical channel thickness for devices with different gatelengths. Also, nanometer-gate MODFETs in AlGaAs/GaAs and InAlAs/InGaAs heterostructures are being fabricated. Both conventional and T-shaped metal gate structures will be investigated for these devices. AlGaAs/GaAs MODFETs with quantum wire channels have been fabricated in heterostructures with high mobilities.

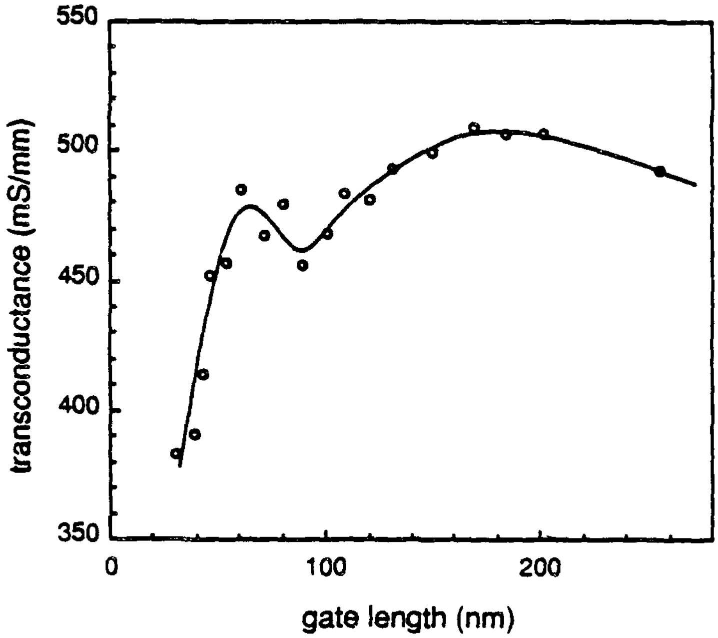
II. Device Characterization

(a) Nanometer-Gate-Length MESFETs

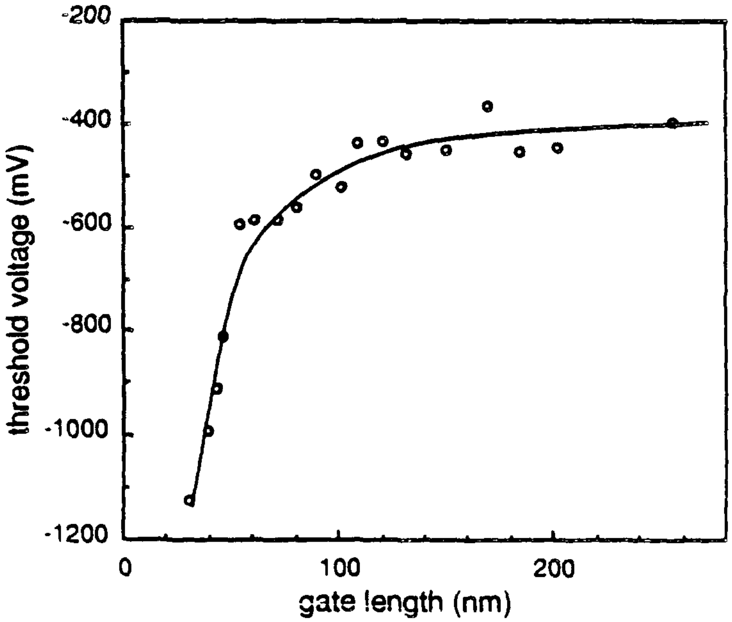
The DC characteristics of GaAs MESFETs have been measured. Figure 1a shows the variation of the extrinsic gm as a function of gatelength. A peak gm of 510 mS/mm was measured for the 160 nm gatelength device at 300 K. This decreased to 450 mS/mm at 90 nm and then appears to rise to a second peak of 485 mS/mm at 60 nm. A dramatic decrease in g_m occurred for devices with gatelength below 60 nm. Short channel effects were manifested in threshold voltage shifts and an increase in subthreshold currents. Figure 1b shows the threshold voltage variation with gatelength. Current efforts are directed at optimizing MESFET and MODFET layers and device layout to optimize DC and RF characteristics. The optimization efforts should lead to the fabrication of high-performance MODFETs with f_T's greater than 300 GHz. These devices will be characterized at room and cryogenic temperatures. Some of this work is a collaborative project with Hughes Research Laboratory, and they have recently provided us with InAlAs/InGaAs/InP MODFET layers.

(b) Quantum Wire Channel MODFETs (QWCFETs)

We have fabricated QWCFETs with multiple quantum wire channels in high-mobility GaAs/AlGaAs MODFET layers. Both wet etching and reactive ion etching have been used to fabricate the channels. The CAIBE method will also be investigated in the near future. The I-V characteristics of QWCFETs have been measured at 300 K and 77 K under light illumination to prevent I-V collapse at 77 K. There were 150 QWs at 0.6 μm pitch with each wire being 0.26 μm in size. An increase in current was observed at 77 K as shown in Figure 2, but no conductance modulation has been observed as yet. Measurements at 4.2 K are imperative to establish quasi-one-dimensional conduction. To this end, we have ordered a Janis Optimag helium dewar with a 9T superconducting magnet and an optical port. This apparatus will allow us to perform variable temperature measurements from 2 K to 300 K. Quantum transport in QWCFETs and nanometer gatelength FETs will be investigated using the new equipment.



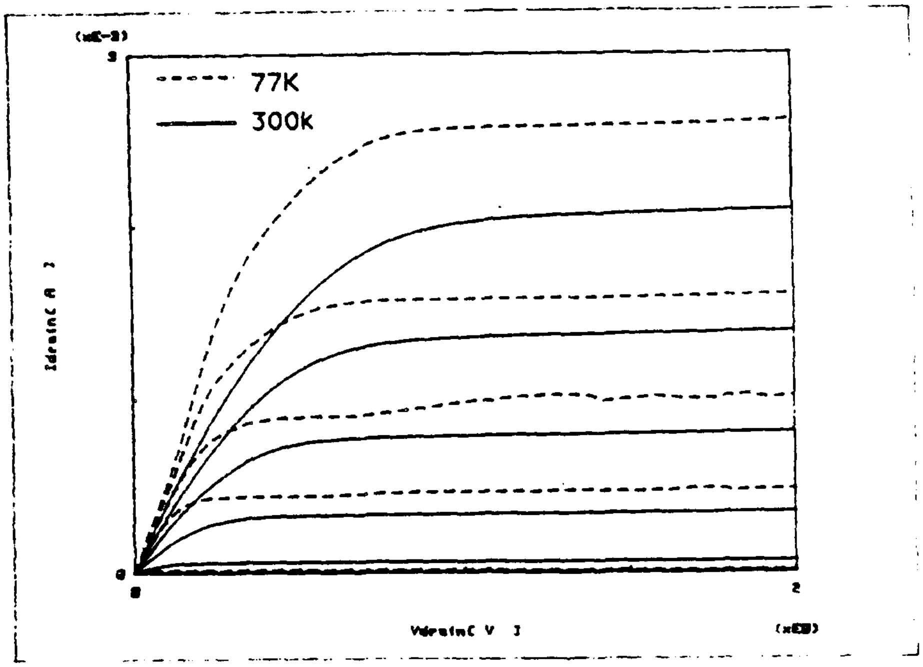
(a)



(b)

Fig. 1. The extrinsic transconductance (a) and the threshold voltage (b) of GaAs MESFETs as a function of the gate length at 300 K. The channel thickness is 250 Å and the channel doping is 4 x 10^{18} cm^{-3}. Each data point represents an average of many devices.

0.6UM 1-D GRATING PITCH FET 300K AND 77K



0.6 µm pitch 1-D FET I-V at 300K and 77K

Fig. 2. I-V characteristics of quantum-wire-channel FET in a high-mobility MODFET layer at 300 K and 77 K under light illumination. Device has 150 wires, each 0.26 μm in size. Further testing will be carried out at 4.2 K.

III. Transport Properties and Simulation of Quantum Wire Structures

We have pursued our theoretical analysis of nonohmic transport properties in quantum wires and paid special attention to transient and spatially varying phenomena. We have implemented the single particle Monte Carlo code to account for spatial nonuniformities in 1D transport, and have also started to develop an ensemble Monte Carlo for treating the effect of carrier-carrier interaction; the latter code provides more flexibility in dealing with spatially dependent processes, such as nonhomogeneous electric fields and confinement fluctuations. Meanwhile, we have incorporated the influence of piezoelectric phonons in our scattering model. Although in 2D modulation-doped structures, carrier screening has been found responsible for an overall suppression of piezoelectric scattering, in the current analysis we have purposely neglected screening effects to investigate the influence of piezoelectric (PZ) scattering on the dynamics of low-energy 1D carriers, with the understanding that the effect of PZ scattering will be somewhat exaggerated. In studying transient and spatially varying phenomena, we have however established that PZ scattering is insignificant for the transport issues described below.

These new modifications allow us to study nonohmic transport in confinement geometries achievable with today's technology. In particular, we have investigated the spatial evolution of 1D carriers from an initial Maxwell-Boltzmann distribution under the sudden application of a longitudinal electric field F_x. The situation is analogous to the injection of carriers in a 1D channel from a bulk region (source) at thermal quasi-equilibrium. At low temperature, the low phonon absorption rate

implies that carrier transport will be essentially ballistic in the 1D channel up to the polar optic phonon (POP) emission threshold, at which point carriers emit a phonon and lose their energy. This process is repeated for several periods until spatial dephasing and randomization by acoustic phonon scattering cause the electrons to converge toward a steady state distribution (Figure 3). The period of the oscillations x_c is given by the simple expression:

$$x_c = \hbar\omega_{POP}/eF_x$$

A similar effect has already been predicted for bulk GaAs although with a weaker intensity due to strong impurity and piezoelectric scattering [24,25]. In 1D modulation-doped structures, we expect the oscillatory motion to be enhanced compared to bulk, mainly because of the absence of angular randomization and the suppression of impurity scattering; in addition, the high peak in the POP emission rate permits relaxation in a quasi-coherent manner. We predict the oscillatory effect will decrease with temperature because the thermal broadening in the initial distribution introduces significant dephasing in the carrier velocity. We have also established that these oscillations exist over an intermediate range of electric fields, only. Indeed, at low field ($F_x < 10$V/cm) transport is dominated by acoustic phonon scattering that smears out the repeated acceleration-POP emission process, whereas at high field ($F_x > 1$kV/cm), the carriers overshoot the POP emission peak and undergo multiple intersubband scattering that suppresses the oscillatory motion.

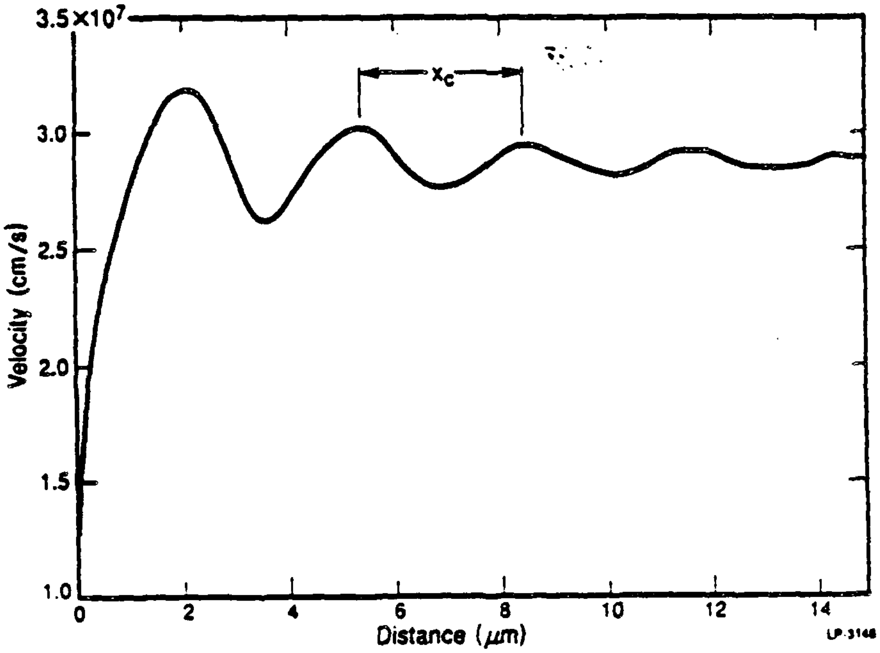


Fig. 3. Electron velocity vs distance in a quasi-1D channel at 77K with $F_x = 100$V/cm. The initial velocity represents the average forward velocity of the initial distribution (Maxwell-Boltzmann).

We are also predicting the occurrence of an anomalous cooling effect in the carrier distribution of quantum wires at high temperature (T>200K). This effect is characterized by the onset of peaks at energy $E = n\hbar\omega_{POP}$ (n is integer) in the distribution function, accompanied by a drop in the average carrier energy $<E>$ below its thermal value kT/2. The cooling only arises in highly confined systems, at intermediate electric field ($500V/cm > F_x > 50V/cm$), and is mostly due to POP absorption and the absence of angular POP scattering. During the cooling process, the thermal energy is converted into drift motion that increases the carrier mobility above the bulk value. We have been able to predict an upper bound of $4X10^4$ cm^2/Vs in the carrier mobility at room temperature for quantum wires with optimum confinement conditions.

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WORK UNIT NUMBER 8

TITLE: Optimum Interconnect Design for High-Speed Digital Applications

SENIOR INVESTIGATORS:

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J. Schutt-Aine, Research Assistant Professor

SCIENTIFIC PERSONNEL AND TITLES:

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P. Harms, Graduate Student
K. Gunawan, Graduate Student
S. Kosanovich, Graduate Student
A. Kouki, Graduate Student
J. F. Lee, Research Associate
K. S. Oh, Graduate Student
R. Palandech, Fellow
S. Schicht, Graduate Student
G. Wilkins, Fellow

SCIENTIFIC OBJECTIVE:

The objective of this effort is to develop electromagnetic modeling of electronic packages with applications in digital and microwave circuits.

SUMMARY OF RESEARCH:

The major aspects of research being pursued in the area of electronic packaging are:

(i) Development of computer-aided design software for the simulation of packages and interconnects

(ii) Investigation of new structures and geometries for high-speed applications

(iii) Development of measurement techniques for high-speed packages

(iv) Development of interactive direct time-domain Maxwell solvers for CAD design

(v) Frequency domain analysis of planar circuits using the finite element method (FEM)

The challenges facing the future designers of the interconnects cannot be met without the availability of accurate and computationally efficient tools for predicting the circuit performance of the networks. With this fact in mind, we have been developing an algorithm called the "scattering parameter method" that has been extensively used in the past for the measurement of high-frequency circuits at microwaves. The main advantages of the scattering parameter approach reside in the flexibility in the choice of the reference system and in the ability of handling both lossless and lossy transmission lines with nonlinear terminations. Moreover, it can conveniently analyze nonuniform transmission lines that find wide applications in microwave and digital communication circuits, e.g, as models for tapered etches in printed circuit boards and tab bonds in chip carrier packages.

Multilayered printed circuit boards and packages often employ orthogonal transmission lines that experience periodic capacitive loading due to the presence of the strips in the adjacent orthogonal layers. The effect of the capacitive loading can be significant and this problem can again be investigated using the scattering matrix analysis. Again, this analysis can be achieved by employing the scattering parameter formulation, and the simulation technique based upon this formulation can also handle nonlinear discontinuities such as diodes and logic gates. We plan to extend this technique in the future to handle nonperiodic irregular discontinuities, as well as coupled transmission lines.

As for the development of Computer-Aided Design Tools, we note that although there are several circuit design programs available for the simulation of the time domain response of lumped networks, these are often inadequate and/or inefficient for distributed networks. For this reason, we have directed our research to the calculation of distributed interconnect parameters from a field solution based on either the frequency or time domain methods for solving Maxwell's equations and the simulation of the time-domain transient response of arbitrary interconnect configurations using the circuit parameters derived from the field solution. Our objective has been to develop a comprehensive approach that combines the calculation and simulation programs into a stand-alone computer-aided design tool for the prediction of electrical behavior of printed circuit boards and packages. In addition, we have been developing interactive programs that provide insights that help the design procedure by displaying real-time visual effects that simulate the changes of current, voltage, and fields in the different parts of the network. Graphical visual effects are being used, for instance, to display the variations of crosstalk signals in coupled transmission lines, and we have recently acquired two powerful workstations to accomplish the visualization task for complex distributed networks.

In addition to the above projects, we have also been investigating some new transmission line configurations for possible applications in interconnect designs. We have demonstrated that the V transmission line, which we have recently developed under the sponsorship of this project, exhibits superior electromagnetic properties when compared to those for the standard microstrips. One reason is because the proximity of the ground plane allows the minimization of stray inductance in situations involving high-frequency device characterization, which also removes the need for plated-through holes for ground access as in the case of the microstrip. In this configuration, most of the fields are confined in the region near air; therefore, it results in a lower effective dielectric constant or faster propagation velocity. A finite element analysis of the structure has been performed and the V-line has been shown to exhibit a lower dispersion characteristic over a wide frequency range. In high-density interconnects, cross-coupling represents the major source of noise as a result of electromagnetic transfer of energy between the neighboring lines. Because of the shielding provided by the triangular ground reference, crosstalk can be reduced using the V-shaped configuration. Theoretical studies indicate that the improvement of about a factor of 7 is gained in the level of crosstalk noise when compared to the microstrip line.

Finally, the determination of the propagation parameters is essential in the design of distributed interconnects, and reliable measurement techniques must be available to verify the validity and the limits of the theoretical calculations. Characteristic impedance and propagation velocity are two important parameters of a single transmission line that can be correlated to the inductance and the capacitance per unit length. Unfortunately, these parameters are all functions of frequency, and characterization at one frequency may often be insufficient. Frequency-domain measurement techniques must, therefore, be developed to obtain a complete characterization. High-frequency effects such as dispersion and losses lead to an ambiguity of the definitions of the basic parameters. Concepts such as wave impedance and propagation velocity are inherent to single-mode propagation and cannot be carried out by a full-wave analysis without revision.

The desired properties of any measurement technique must include accuracy, repeatability, and consistency with other means of characterization. These properties may explain the existence of a multiplicity of approaches associated with the measurement of a given parameter.

Several measurement techniques have been developed at the Electromagnetic Communication Laboratory for the characterization of high-frequency interconnects. Presently, three major areas in measurement techniques are under intensive study in the course of this project.

Skin effect as a result of finite strip conductivity is a high-frequency phenomenon that is more prominent in thin film interconnect structures. The analysis and modeling of the skin effect have been fully addressed; however, the experimental characterization remains a tedious task due to interaction of other high-frequency effects such as dispersion, attenuation, and higher-order mode propagation. Isolating the skin effect from measurements cannot, therefore, be made without a sufficiently accurate high-frequency model for strip transmission lines. It is the goal of this project to implement the simplest high-frequency model that allows the determination of the parameters of interest. Subsequent levels of complexity can be added as frequency is increased to measure trends and dependence with frequency.

Dielectric characterization is useful in determining the propagation properties of a medium. This characterization involves the measurement of the complex permittivity of a dielectric that consists of a dielectric constant and the loss tangent. Several techniques have been used for the measurement of the dielectric constant, but the need still exists for a method that combines convenience and accuracy. The method used in the Electromagnetic Communication Laboratory consists of measuring the scattering parameter response of a piece of dielectric material with a conductor on both sides. From the resonance curves and the knowledge of the normal modes of the so-defined cavity, the dielectric constant can be extracted. The accuracy of this method is limited by wall losses and radiation. More recently, the HP85070 dielectric probe has been introduced for the measurement of the dielectric constant on a network analyzer and a unit is being evaluated in the laboratory; accuracy on the order of 5% can be obtained up to 18 GHz. The advantages of the method are the accuracy and the readiness of the dielectric constant from the measurement.

The measurement of the dielectric loss tangent poses more serious challenges. Since the accuracies of most network analyzers are in the order of a few percent, the loss tangent of low-loss materials in the order of 10-3 and lower cannot be determined using scattering parameter measurements. A cavity method based on the measurement of the quality factor at resonance is more amenable; however, such a method will require the use of a more sophisticated test setup and probing techniques.

The determination of package and chip carrier inductance is important in determining their range of usefulness. Until recently, most chip carriers consisted of structures in which the lead frame occupied nearly 80% of the total area leading to pin inductances of very large values. More generally, because package and chip carrier lead frames make up networks of sufficient complexity, the analysis deserves very special attention.

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WORK UNIT NUMBER 9

TITLE: High-Performance Computer Architectures

SENIOR INVESTIGATORS:

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SCIENTIFIC PERSONNEL AND TITLES:

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SCIENTIFIC OBJECTIVE:

This unit seeks to develop, model, and analyze efficient computer architectures that will exploit semiconductor technology to deliver high performance for important applications. High-density technologies such as CMOS VLSI have provided high-performance, low-cost computation elements for parallel processing systems. To achieve high performance, the nature of important applications must be characterized to provide insights into how compilation and hardware techniques affect the performance of parallel processing systems. We will address two major aspects: processor/system architectures and memory architectures. In both cases, we will develop integrated architecture, compilation, and analysis methodologies to achieve high performance for important military, scientific, and engineering applications.

SUMMARY OF RESEARCH:

Processor/System Architectures

We have developed a low overhead method for instrumenting the structure and dynamic behavior of parallel Fortran programs. Our method allows collecting information about available parallelism and granularity in these programs. We have also developed a simulation tool to investigate the synchronization and task management issues in executing parallel programs on shared memory multiprocessors. We have designed efficient synchronization and task management algorithms and have implemented them in our simulation tool. We evaluated the performance implications of these algorithms using different hardware synchronization primitives on real programs.

Our early results showed that even for multiprocessors with a moderate number of processors (8 to 16), the choice of the hardware synchronization primitive has substantial impact on program execution time. We have identified loop scheduling overhead as a major source for performance degradation. In our simulation model, we quantified this overhead for the synchronization primitives test&set, exchange-byte, and fetch&add, in addition to a synchronization bus that supports atomic lock/unlock operations. The major components of overhead are memory contention in implementing lock/unlock operations and the speed of transferring lock ownership from one processor to another. The synchronization and task management algorithms heavily use shared counters for processor communication, and we observed that hardware support of the fetch&add primitive eliminates most of the lock/unlock operations needed in their implementation. Experiments with real programs showed that, without machine-dependent program optimizations, supporting proper hardware

synchronization primitives results in substantial speed-up: We found that use of the test&set primitive severely degrades performance, where an exchange-byte primitive can be used efficiently for programs with medium loop granularity (loop iterations with 200 or more instructions). Support of a fetch&add primitive was found to be as efficient as implementing atomic lock/unlock operations with a synchronization bus. In both cases, parallel loops with granularity of 100 instructions could be executed efficiently.

The analysis of the dynamic behavior of real applications showed that granularity of parallel loops varies between 20 to 1000 instructions, and parallelism may exist in the form nested parallel loops. In our research, we are continuing to investigate more aggressive loop scheduling algorithms for efficient execution of loops with small granularity. We are also exploring the possibility of exploiting the parallelism in nested parallel loops to overlap synchronization overhead with useful work.

Memory Architectures

We have continued to develop our low-cost method for trace-driven simulation and have been applying the methodology to evaluate memory organizations for high-performance computer systems. Our method involves sampling the execution trace of programs and using these *sampled traces* for trace-driven simulation. This approach allows address traces from the execution of real numerical programs to be used in our experiments. Evaluation has so far concentrated on the performance and behavior of cache memories in single and multiprocessor vector processors.

Our previous cache results show that cache memories can be effective in a vector processor, but the vector stride distance can cause dramatic and unpredictable cache behavior. This behavior makes parameter selection in vector cache designs more difficult than parameter selection in cache designs for general purpose machines. For example, in a vector cache the best performance at a particular cache block size for one program may result in the worst performance for another program. Our experiments show that prefetching data into a cache, after a cache miss, can reduce this unpredictability. Two simple prefetch schemes, *sequential-prefetch* and *stride-prefetch*, have been proposed. Both schemes adapt the data size loaded or prefetched into the cache to the reference type. The sequential-prefetch scheme loads multiple consecutive data blocks into the cache if a reference is a scalar or a vector access with a small stride distance. A vector access with a large stride distance loads a single data block to minimize the fetching of unused data into the cache. The stride-prefetch scheme trades off the cache hit ratio with data fetching by always prefetching multiple data blocks using the stride information. These two prefetch schemes have been shown to have better performance than a no-prefetch cache in a vector processor system.

Cache memories may offer a cost-effective solution to the high bandwidth requirement of vector multiprocessors. Block size selection for multiprocessor cache memories have additional complexities specific to systems with more than one processor. A large block size can reduce the number of misses in an individual cache, but this can be offset by increased data invalidations in maintaining cache coherence among multiple caches. The use of a large block size also increases memory traffic. In a system with a shared memory interconnect such as a bus, this can quickly lead to resource saturation. However, a small block size can result in similar high-memory usage because of an increase in cache misses. Our initial results show that the proposed prefetch schemes can be effective in vector multiprocessor cache memories. By using a small block size, the data size invalidated by cache coherence maintenance can be minimized; and by prefetching multiple data blocks, cache misses can be reduced.

Our research will continue to investigate the prefetch schemes and the memory organizations to support these prefetch schemes.

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WORK UNIT NUMBER 10

TITLE: Fault-Tolerant Parallel Computer Systems

SENIOR INVESTIGATORS:

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SCIENTIFIC PERSONNEL AND TITLES:

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SCIENTIFIC OBJECTIVE:

This unit will explore concepts in reliable computing that will provide an understanding of the basic principles in design and analysis of reliable VLSI-based parallel computer architectures. As advances in integrated circuit technology continue, the resulting complexity in the systems developed require new approaches for realizing reliable and fault-tolerant systems. There is an increasing need for systems that will continue to function under a variety of workload environments and failure conditions. We have identified three issues that require particular attention from both technology and systems viewpoints. Basic research will be performed in the specific areas of reconfiguration for fault tolerance in parallel architectures, recovery from errors in parallel architectures, and the development of realistic models to describe the dependability of parallel computer systems.

SUMMARY OF RESEARCH:

Reconfigurable Parallel Architectures

In the past year, we have continued research into the investigation of hardware- and software-based reconfiguration strategies for message-passing parallel architectures. Previously, we had studied three schemes for reconfiguration in hypercubes, two in hardware, and one in software [1]. The hardware schemes used cost-effective embeddings of spare processors in the system with optimal reconfiguration and rerouting strategies for hypercubes. This year we have extended the theory for mesh-based multiprocessors, and we have developed a stronger theoretical basis for the embedding. The software scheme requires no hardware modification and is based on the notion of reconfiguration using virtual processors. This strategy has been applied for hypercube and mesh-based systems. We have also investigated several routing strategies for hypercubes and meshes under faults [2].

We are currently developing an experimental environment to study reconfiguration and rerouting strategies and load balancing under failures using a CSIM-based simulation environment. Using this, we plan to investigate and evaluate the cost/performance trade-offs in various schemes using analysis and simulation [3]. We are planning to use a recently developed trace-gathering system for parallel applications on the hypercube to generate statistics on computational and communication requirements to evaluate the performance degradation of actual parallel applications. We are also in the process of evaluating our software-based reconfiguration scheme on the Intel iPSC/2 hypercube.

Error Recovery in Parallel Architectures

In the area of error recovery for parallel architectures, we have made specific progress concerning the use of compiler technology in determining checkpoint placement and in assisting in multiple instruction retry [4-6] and recovery through graceful degradation [7,8].

We have completed the experimental evaluation of our compiler-based approach to generating efficient full checkpoints for process recovery [4,5]. Our approach to full checkpointing is programmer, operating system, and hardware transparent. Compile-time information is exploited to maintain the desired checkpoint interval and to reduce the size of checkpoints. Compiler-generated sparse potential checkpoint code is used to maintain the desired checkpoint interval. Adaptive checkpointing has been developed to reduce the size of checkpoints by exploiting potentially large variations in memory usage. A training technique is used in selecting low-cost, high-coverage potential checkpoints. These compiler-assisted checkpointing techniques have been implemented in a modified version of the GNU C (GCC) compiler, and experiments measuring performance costs have been completed.

We have also derived initial results concerning the use of compilers for multiple instruction retry for rapid recovery from transient failures [6]. Our technique provides a flexible software-based approach to instruction retry. The multiple instruction retry capability is achieved by having the compiler remove all forms of instruction anti-dependencies for the number of instructions that will potentially be re-executed. The anti-dependencies are removed in the pseudo code by using loop protection, loop expansion, and node splitting. The anti-dependencies are removed at the level of the machine registers by enforcing anti-dependencies in the register allocator's interference graph.

Our final area of progress in the last twelve months has been the development of graceful degradation techniques for distributed memory architectures [7,8]. We have completed the experimental evaluation of a gracefully degradable method of distributed garbage collection [8]. We have also evaluated our technique for graceful degradation on hypercube architectures. CPU-bound hypercube programs using our second-order parameterized data-distribution technique can run on a group of cubes of any size to achieve graceful degradation without recompilation. A transmission mechanism has been designed to switch the performance of a second-order parameterized data-distribution hypercube program to that of a corresponding first-order program when the latter is superior. A package of procedures has been implemented on the Intel iPSC/2 hypercube to support the approach.

Modeling and Measurement of Computer System Dependability

In the last year, we continued our study of dependability evaluation and modeling for multicomputer systems based on a set of error data collected from a DEC VAX cluster. By our previous results, correlated failures and software errors are two prominent dependability issues in the measured systems. Our research concentrated on these two issues. First, we conducted a correlation analysis to quantify relationships between errors/failures on the different VAX machines. Then we investigated the impact of correlated failures on availability and reliability estimates. We also started to address issues of model construction for systems with correlated failures. For software errors, we performed a detailed analysis on the software error data.

Results of correlation analysis show that errors are highly correlated across machines (average correlation coefficient $\rho = 0.65$) due to sharing of resources. The measured failure correlation coefficient, however, is not high (0.15). Based on the VAX cluster data, it is shown that models that ignore correlated failures can underestimate unavailability by orders of magnitude. Even a small correlation significantly affects system unavailability. A validated analytical model, to calculate availability of simple systems with correlated failures, is proposed. Similarly, reliability is also significantly influenced by correlated failures. The joint failure rate among components, λ_f, is found to be the key parameter for estimating the reliability of systems with correlated failures. A validated relationship between ρ and λ_f for the 1-out-of-2 system is derived.

Results of software error analysis show that software errors have the lowest recovery probability (0.11) among all errors. Most software errors are control problems (such as "unexpected system service exception"). The availability of the VAX/VMS operating systems running on the seven VAX machines is evaluated to be 0.99954 for 250 days of operation.

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WORK UNIT NUMBER 11

TITLE: Efficient Computation Techniques

SENIOR INVESTIGATORS:

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SCIENTIFIC OBJECTIVE:

The analysis and design of efficient computation techniques has been for several years one of the most vigorous areas of research in information processing. Its impact has been not only on the availability of better computational methods for a number of significant applications, but also on the awareness both in the computing community and in the users' community of the crucial importance of algorithmic design. By investigating both upper and lower bounds to the resource requirements of specific applications and by developing effective methods for designing parallel VLSI algorithms, this discipline effectively develops a methodology aiming at a quantitative formulation of the inherent difficulty of problems in technology-driven computational systems.

The involvement of our research group with this topic is well established and dates back to the early seventies. Our record over this period shows that our focus (as well as that of our peer community) has been adjusting dynamically, as evolutions in technologies continuously modify the general research horizon and the perception of relevance. The most significant development of this type has been the advent of Very-Large-Scale-Integration (VLSI), which has profoundly influenced essentially every facet of our current research interests. The advent of VLSI is important in two major respects: one is the present possibility to realize massively parallel computers; the other is the introduction of criteria of complexity (the VLSI "model") that takes into account the design rules dictated by current technology.

Thus, parallel computation is, again, the dominant theme of the research outlined in this proposal, with particular emphasis on applications that are significant for JSEP. This research interest, of course, will not entirely replace our traditional interest for conventional serial computation, with which it constructively and productively interacts. In fact, the study of serial algorithms benefits the development of parallel algorithms, either because of direct parallelizability or because of the obtained insights on the structure of specific problems.

SUMMARY OF RESEARCH:

In the past year, we have studied two important areas of parallel computation that contribute to our overall objective of this research, namely, mapping algorithms on parallel processors and designing efficient parallel algorithms. In the area of mapping algorithms, we have studied the mapping of recurrences, neural-network simulations, and circuit placement and routing on VLSI array processors and multiprocessors. In the design of parallel algorithms, we have studied efficient algorithms to determine the connected components of a graph and the limitations of digital filtering from a VLSI perspective.

In mapping recurrences to VLSI array processors, we studied the isomorphicism between the parameter method we proposed for mapping uniform recurrences on VLSI systolic arrays and the dependence method proposed by Moldovan and Fortes [1]. We extended our original parameter method beyond the mapping of two-dimensional uniform recurrences on one- or two-dimensional

systolic arrays. The new method can map any N-dimensional uniform recurrences to lower dimensional array processors and is capable of mapping a limited set of nonuniform recurrences [2]. We applied the above method to mapping two-dimensional digital filters on one-dimensional array processors [3] and studied algorithms for mapping under limited input/output pins [4].

In mapping neural-network simulations to multiprocessors, we studied the optimal mapping of multilayer feed-forward artificial neural networks on message-passing multicomputers [5,6]. Our objective is to minimize the completion time of simulating neural networks in parallel on multicomputers. We developed a novel approximation algorithm for mapping large neural networks, given a user-specified error degree that could be tolerated in the final mapping. The proposed algorithm can map neural networks of thousands of neurons to within a user-specified error degree. We studied both static and dynamic mapping schemes for systems with static and dynamic background workloads.

In mapping algorithms for circuit placement and routing on multiprocessors, we developed a theoretical model that characterizes the relationship between the best solution (incumbent) found by an iterative algorithm (simulated annealing) and the time spent in achieving it [7]. The model was used to achieve a trade-off between solution quality and time spent. This gives an idea of the time that the iterative algorithm should be terminated when the marginal gain in solution quality is smaller than the marginal increase in cost (or time) spent. Nonlinear regression analysis was used to predict the decrease in time with respect to improvement in solution quality. Experimental results on benchmark circuits were presented to show the errors of run-time prediction as compared to a static prediction. The method adopted is very general and can be extended to a variety of applications that use iterative algorithms. We are in the process of extending this theoretical model when the mapping algorithms are carried out on parallel processors.

In the area of designing efficient parallel algorithms, we adopt an approach of first designing the algorithm on a widely accepted model of computation, the parallel random access machine (PRAM), and extending the resulting algorithm to more realistic physical models. Used by numerous researchers around the world, the PRAM provides a particularly convenient conceptual framework for the study of parallel algorithms. Under previous JSEP support, we have successfully designed and analyzed numerous PRAM algorithms. However, the PRAM assumes that all processors are synchronized and take steps simultaneously. Since signal propagation delays cause clock skew, rigid synchronization is physically impossible. Thus we have begun to investigate a much more realistic model of parallel computation, the asynchronous PRAM (APRAM). To explore capabilities of this model, we have designed two algorithms to determine the connected components of a graph [8]. One algorithm runs on an APRAM with only atomic **read** and **write** primitives and requires at most $O(n \log n)$ rounds, where n is the number of vertices. The other algorithm runs on an APRAM with limited **read-modify-write** primitives and requires at most $O(\log n)$ rounds. Other researchers have designed asynchronous parallel algorithms for finding connected components, but their algorithms use either randomization or unrealistically powerful memory access primitives. In contrast, our algorithms can run on computers constructed in currently feasible technologies.

Last, we investigated the theoretical behavior of digital filtering implemented using the evolving VLSI technologies. We have made significant inroads into the analysis of digital filtering from a VLSI perspective, i.e., from the viewpoint of combined resource utilization, such as time, space, and memory. We have begun with the investigation of memory requirements of digital filters as determined by filter parameters and desired accuracy and have developed a full analysis for first-order filters. The main feature of this investigation is that lower bounds are obtained with no structural assumption on the finite-state machine selected to approximate the ideal filter. Two specific realizations are discussed: a classical state-roundoff implementation and a higher order FIR approximation. Upper and lower bounds on memory requirements are also shown to be in remarkable agreement. These results are currently being prepared into a manuscript for submission.

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WORK UNIT NUMBER 12

TITLE: Computer-Aided Design of Very High-Speed Integrated Circuits

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SCIENTIFIC OBJECTIVE:

Computer-aided design of integrated circuits has been the subject of many research activities for a number of years, both in universities and industry, and many CAD tools have been developed to aid in the design and analysis of integrated circuits and systems. However, there are still many basic issues that must be resolved as the processing technologies evolve and device feature sizes shrink. To manage the increasing complexity of VLSI designs, hierarchical techniques are employed. At each level in the hierarchy, the design is often guided by an attempt to minimize a certain cost function satisfying a set of constraints. The need for developing efficient CAD tools to produce optimum designs is becoming more apparent, particularly for high-performance custom or semi-custom chips. Automatic synthesis techniques that produce optimized designs from higher level specifications are needed. For example, synthesis techniques that minimize the number of devices needed in implementing functional specifications would be desirable. At the same time, the design needs to be easily testable and reliable. The performance of the design in terms of area and speed needs to be optimized. Different design styles offer different trade-offs between area and speed. The effect of interconnect parasitics on speed is becoming more important as feature sizes shrink. Thus, designs that use two or more metal layers of interconnects are becoming viable techniques to improve speed.

Other important issues that must be addressed include chip reliability, both short and long term, and chip yield. These require the development of statistical analysis techniques. Statistical analysis is essential in order to insure that fabricated integrated circuits would meet performance specifications with a reasonable yield. The random nature of process variations makes it difficult to predict the distribution of performance statistics and hence the chip yield, unless the design is carried out by using the so-called worst-case analysis. In practice, the worst-case analysis is often used mainly because it guarantees that almost all functional devices would meet parametric specifications. However, the worst-case analysis imposes too much of a burden on the process development and is often overly pessimistic. The state-of-the-art design should take advantage of new technologies and hence requires in-depth statistical analysis to make the design robust to process variations as much as possible. This does not mean that statistical design methods alone can solve the yield problem. Rather, the statistical design approach treats the variations in circuit performances as noise and attempts to find an optimal design that provides a good yield.

The objective of this proposed research is to develop analysis and design automation techniques for reliable high-speed integrated circuit designs. This includes the automatic synthesis of testable circuits with a reduced number of devices, automatic generation of layout using two metal interconnects, and the development of mathematical methods and algorithms for optimizing the design. The work will also include the development of rigorous and systematic statistical design techniques that are computationally efficient and hence applicable to the design practice of VLSI circuits or exploratory development of high-performance integrated circuits.

SUMMARY OF RESEARCH:

During the past year, we have been working mainly on topics in design verification and in reliability analysis. In the area of design verification, we have worked on a number of projects at various levels in the design verification process of VLSI circuits; namely, circuit, timing, logic, and mixed-mode simulation.

At the circuit level, we have developed parallel solution algorithms for sparse linear systems on a vector multiprocessor computer. The algorithms employ nested decomposition techniques and are targeted for use in parallel circuit simulation [1]. The algorithms have also been adapted to run on message-passing computers solve systems with block tridiagonal or banded matrix structures [5]. We have also studied the implementation of relaxation-based algorithms for circuit simulation on multiprocessors [4]. The implementation has been done mainly on an Alliant FX/80 multiprocessor computer with eight processors in the Center for Computer Research and Development at the University of Illinois, Urbana-Champaign.

As the size and complexity of integrated circuits increase, the trend is to mix both analog and digital circuits on the same chip. Thus, mixed-signal simulation techniques are needed. In this respect, we have developed mixed-mode simulation techniques that include circuit, timing, and logic simulation with assignable delays [2,3,7,17]. The techniques have been tested on a number of mixed analog/digital circuits obtained from industry.

We have also implemented fast logic simulation techniques with assignable delay using bit-wise operations and parallel processing [3]. The program has been run on the Alliant FX/80. In addition, we have developed a new matrix algebra for logic simulation of MOS circuits using switch-level modeling techniques [12,16]. We have applied the technique for efficient transistor-level fault simulation [6]. This new approach allows realistic fault models, such as bridging faults and transistor stuck-open and stuck-on faults with variable strength without sacrificing computational speed. Current testing is also included in a natural way to increase fault coverage. We have also studied the complexity of test generation for transistor-level faults [11].

In the area of design for reliability, we have continued our work on the new probabilistic simulation approach [10,15]. An improved derivation of expected value and variance current waveforms drawn by CMOS structures during switching has been obtained. The new method gives more accurate results compared to our previous method and adds more credibility to our probabilistic simulation approach [18]. The new method is being implemented in a hierarchical simulator. In addition, efficient computational algorithms have been implemented to compute the expected value and variance current densities in the bus for electromigration estimation and bus resizing [19]. The circuit model of the bus could be very large and circuit reduction combined with sparse matrix solution techniques have been applied for efficient and fast solution. A system for electromigration estimation that includes extraction, probabilistic simulation, and expected current density in the bus has been developed [13].

The present state of the VLSI is such that a monolithic VLSI CPU or DSP chip contains more than one million transistors and the packing density is steadily increasing. In the case of a DRAM chip, the packing density is almost quadrupled. One of the most difficult problems in handling the increasing design complexity lies in the timing verification of the entire chip. Even with

supercomputers, detailed circuit-level simulation cannot be adequately handled. As a result, the timing verification of digital VLSI chips has resorted to fast timing simulation packages for more than a decade.

The conventional timing simulation programs had to use rather crude models of transistors or circuit primitives in order to reduce the computation time at a significant sacrifice of simulation accuracy. As a result, most existing timing simulators can miss an entire cycle or more due to the accumulation of errors in multiple cycle simulation of VLSI circuits. Even with a sacrifice of accuracy, the timing simulation of very large circuits can still take an excessively long time, especially for state-of-the-art VLSI chips let alone circuit-level simulation problems. The recent activities on parallel simulation further reduce the simulation time by using a multitude of processors for circuit or timing simulation with proper circuit partitioning. Some success has been achieved to reduce simulation time by a factor almost equal to the number of processors used. However, interprocessor communication problems can become more pronounced as the number of processors is increased; and thus it is not clear whether a drastic speed-up can be achieved by using parallel simulation alone.

In order to address this serious problem in timing verification of digital MOS VLSI circuits, we have researched a new timing simulation approach that takes a drastically different formulation of the problem. Recently, we have successfully developed a new timing simulation program, ILLIADS (Illinois Analogous Digital Simulator), which contains over 30,000 lines of codes in C programming language. To highlight its salient features briefly, it can decrease the simulation time over SPICE-generation programs by a factor of 3N, where N is the number of transistors to be simulated. In other words, for a circuit containing, for example, 100,000 MOS transistors, ILLIADS can speed up the simulation time over SPICE or its derivative programs by 300,000 times with much better accuracy than any other timing simulation program. As far as we know, these achievements are superior to other timing simulators in both speed-up and simulation accuracy.

This drastic improvement has been made possible through the introduction of a new generic circuit primitive and a new rigorous analytical solution of nonlinear differential circuits equations, i.e., Riccati equations, under MOS circuits and analytical solutions. We have avoided the traditional numerical integration steps to remove time-consuming iteration loops and also to reduce numerical errors. Essentially, ILLIADS takes in piecewise linear input waveforms as specified by users along with a netlist in SPICE-like format and produces analogous output waveforms virtually identical to SPICE outputs with 3N speed-up, where N is the number of transistors in the given netlist. We have been able to simulate a digital MOS circuit containing 235,000 transistors in less than 10 minutes on a workstation with about 80Mbytes of swapspace. The estimated speed-up is almost one million. It remains as an estimate, since SPICE cannot handle such a large circuit. The simulation time is expected to go down even further on a bigger dedicated machine. This, we believe, has never been achieved before especially on a workstation. Further research and development of ILLIADS should enable accurate simulation of digital MOS VLSI chips and even multichip modules (MCMs) with affordable computation time.

The current version of ILLIADS has already been used effectively in class projects (ECE482, Physical Design of VLSI, Spring 1991) and also for reliability simulation. For reliability simulation of hot-carrier-induced circuit performance degradations, we have implemented damaged MOS transistor models into ILLIADS-R, a reliability simulator derived from ILLIADS, and used ILLIADS-R to simulate and analyze long-term aging phenomena of MOS VLSI circuits containing as many as 3,700 transistors, which is again a first-time achievement anywhere. Due to the added complexity, the reliability simulation usually takes much longer than the timing simulation. The development of physical models and algorithms for reliability simulation has been funded by the Semiconductor Research Corporation (SRC) and the Rome Air Development Center (RADC). It was a very timely and almost perfect linkage between ILLIADS and the reliability simulation projects. Another interesting application is to apply ILLIADS for mixed analog-digital circuit simulation. Since ILLIADS outputs analogous voltage waveforms, its interface with detailed circuit simulators like SPICE for analog simulation is natural and would not suffer from the signal mismatch problems faced by most mixed-mode simulators.

Our research accomplishment is another good example of how JSEP research results of a high-risk project have been fanned out to impact other research projects. It was a high-risk project in view of peers who had initial doubts on our approach. We have received several requests for the release of the ILLIADS program to industry and universities and plan to distribute it for beta-site testing near the end of this summer. The initial results of this ILLIADS project will be presented at the 1991 IEEE/ACM Design Automation Conference at San Francisco in June. Two journal papers and one additional conference paper have been submitted for publication.

A general digital circuit may be treated as a collection of combinational subcircuits that lie between latches. To satisfy a given clocking requirement for the circuit, it must be ensured that each combinational subcircuit takes its inputs from a set of latches at the time of a clock transition and produces valid signals at its set of output latches before the next clock transition. In order to do so, the sizes of certain transistors in the circuit need to be increased to more than the minimum allowable size. This may, however, make the area intolerably large; hence, a set of transistor sizes that gives a satisfactory trade-off between the area and the delay must be found. This leads to the transistor sizing problem, for each combinational stage, of minimizing the total area subject to a delay constraint for that stage. In addition, all transistor sizes must be at least the minimum size allowed by the process technology.

During the past year, under JSEP sponsorship, we have implemented a computer program called CONTRAST (Convex Optimization-based Novel TRAnsistor Sizing Tool) for solving the transistor sizing problem. CONTRAST uses a relatively sophisticated waveform-independent delay estimator to find the delay through the circuit. It recognizes the fact that rise and fall delays may be different and accounts for this while computing the overall delay through the circuit. The delay estimator attempts to identify the transistors in the circuit that contribute to the worst-case (over all possible input waveforms) rise or fall delay at the outputs. General pass transistor networks, including those containing bridges, can also be handled. In this approach, both the circuit delay and area are modeled as *posynomial* (polynomial with positive coefficients) functions of the transistor sizes. A simple variable transformation is then used to transform posynomials to convex functions. CONTRAST then uses an accurate and efficient algorithm [50] for minimizing a convex objective function over a convex domain. The algorithm starts by bounding the convex domain by an initial polytope. By using special cutting plane techniques, the volume of this polytope is shrunk in each iteration, while ensuring the optimal solution lies within the boundary of the polytope. The iterations stop when the volume of the polytope becomes sufficiently small. CONTRAST has been run on a variety of combinational circuits, and initial results indicate that it consistently gives a significantly lower area for a given delay specification when compared with TILOS [51,52].

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WORK UNIT NUMBER 13

TITLE: Adaptive Systems for Identification, Filtering, and Control

SENIOR INVESTIGATORS:

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SCIENTIFIC OBJECTIVE:

Our major goal is the fundamental understanding of how to design high-performance and robust adaptive systems for use in control, filtering, estimation, and identification.

Adaptive systems are comprised of algorithms that utilize information acquired on-line to modify the system. The goals of this modification are several. First, the resulting system should be stable. Second, by fine tuning the controller on-line, using the most recent data to model the system, the performance of the system can be optimized.

The basic component of all adaptive algorithms consists of a parameter estimator, the most common one being based on least-squares. The fundamental behavior of such least-squares algorithms, in particular their stability and convergence performance, is a basic and most important issue about which little is known. Some very recent results obtained by us exhibit the promise of providing a broadly applicable analysis of least-squares estimation algorithms in a variety of environments.

A second issue of interest is the *self-tuning* properties of adaptive systems; i.e., will adaptive systems automatically tune themselves to optimal controllers? We intend to investigate the self-tuning property of the minimum variance regulator as well as its generalizations and predictive control algorithms.

A third issue of importance is the *robustness* of adaptive controllers. Since adaptive controllers and estimators are highly nonlinear stochastic systems, their stability can be adversely affected by unmodeled dynamics and disturbances. A sound understanding of such instability phenomena, as well as safety fixes, is essential. In this regard, we will investigate a promising novel approach to robust adaptive control. Our approach essentially attempts a synthesis of H^{∞}-optimal control with adaptive feedback strategies. This scheme is particularly appropriate for treating the effects of unmodeled dynamics and exogenous disturbances.

A key reason for using "adaptation" is to automatically tune the behavior to match slowly drifting, time-varying systems. We will examine the stability and performance issues involved in such tracking problems.

Lastly, adaptive control is beginning to make the crucial transition from applicability to linear plants only to applicability to fundamentally nonlinear systems. Though such nonlinear environments introduce their own set of design issues, they also allow quicker parameter convergence due to the "excitation" introduced by nonlinear elements. Our goal will be to develop an applicable theory of nonlinear adaptive control.

SUMMARY OF RESEARCH:

Adaptive control algorithms can broadly be divided into two categories—those based on "parallel model" methods and those based on "extended least squares" methods. In the area of parallel model adaptation, we have developed new algorithms for the problem of adaptive active noise cancelling, as well as adaptive feedforward control. The former is a two-microphone based system, for which the university has applied for a patent. In addition to working out the theory for these algorithms, we have also theoretically analyzed the output error identification and adaptive IIR filtering algorithms, both of which have been open areas since about 1976.

For extended least-squares-based algorithms, we have developed the convergence theory for adaptive filtering, prediction, and control. In particular, we have developed adaptive algorithms based on a generalized certainty equivalence principle. Also, we have resolved the self-optimality of noninterlaced algorithms for multiple delay systems.

For about a decade now, the problem of designing robust adaptive controllers has been an intense area of activity. We have recently shown that by simply confining the parameter estimates to be in a compact convex set containing a nominal approximation to the true system, we can establish robustness of continuous time adaptive controllers with respect to both bounded disturbances as well as small unmodeled dynamics. We have also generalized such a result to the extended least squares algorithm.

In addition to these results, we have obtained two other important results in adaptive and robust control:

(a) We have addressed the problem of synthesizing admissible controllers that simultaneously provide robust regulation and reduce the norm of a certain closed-loop transfer function. Several important problems fall into this general framework; for example, designing controllers that provide tracking robustly against the maximal amount of modelling uncertainty. The requirement of robust tracking, as is well known, leads to requiring an internal model of the exosystem in the feedback loop. One may then incorporate this model into the generalized plant and solve an H_∞ optimal control problem. However, this approach fails as the resulting Riccati equations do not admit solutions. We have developed an alternate approach that circumvents this problem, and we are able to provide computable necessary and sufficient conditions for our problem to admit a solution as well as explicit state-space formulae for a certain "central" solution.

(b) In what promises to be an exciting development, we have recently been able to solve certain time-domain model-validation problems. The general model-validation problem is as follows: given an a priori model for a physical plant (for example, consisting of a nominal plant model, a noise-model, and uncertainty bounds) together with time-domain input-output data, determine whether or not the input-output data record is consistent with the model. Previous approaches to model-validation have resulted in computationally intractable problems and have not been able to explicitly incorporate the requirement of causality in the unmodelled dynamics. We have been able to present computable solutions to the model validation problem under a variety of modelling hypotheses ranging from coprime-factor uncertainty to the general feedback structured uncertainty of Doyle. We have employed the techniques of this work to develop a novel method for robust identification of which least squares is a special case. The solution of many of these problems reduces to convex programming.

Until a few years ago, adaptive linear and geometric nonlinear methods belonged to two separate areas of control theory. Recently, the problem of adaptive nonlinear control was formulated to deal with the control of plants containing both unknown parameters and known nonlinearities. A realistic plan of attack for this challenging new problem led through a series of simpler problems, each formulated under certain restrictive assumptions. In the last year, we obtained new results that advanced in several directions our ability to control nonlinear systems with unknown parameters. These results are based on new and conceptually simple step-by-step design procedures that interlace, at each step, the change of coordinates required for linearization and the construction of update laws

required for adaptation. Using these procedures, we were able to remove many of the restrictive assumptions of previously available results, including the often unrealistic assumption of full-state measurement.

In the area of distributed scheduling, which is important to several applications such as semiconductor manufacturing, we have established the stability of several due date and buffer priority based scheduling algorithms. Two schemes are especially promising. The Last Buffer First Serve algorithm exhibits low mean delays in simulations, while the Least Slack algorithm exhibits low variance.

In the area of learning, we have obtained sufficient conditions and also necessary conditions for the ability to learn an entire family of concepts from just one simulation. This establishes a close link between the areas of estimation and learning.

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WORK UNIT NUMBER 14

TITLE: Decentralized, Distributed, and Robust Systems

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SCIENTIFIC OBJECTIVE:

Advances in communications and computer engineering, together with the recent developments in solid state sensors technology, provide the opportunity for *decentralized* and *distributed* control of large dynamic systems, using distributed information processing. Typical large dynamic control systems problems include flexible aircraft control, ship steering, vibration and control of large flexible space structures, and remote control and navigation of all-terrain vehicles. Distributed control of such systems exploits the dynamic response characteristics of materials and solid state sensors, processors, and actuators for combined passive and active control configurations. Such systems utilize locally generated process measurements together with local control inputs to obtain satisfactory global dynamic response characteristics in the presence of system modeling uncertainties (including unmodeled dynamics) and disturbance inputs.

Decentralization means that each local controller uses only part of the available information, and the **distributed** nature arises because the overall task of controlling the large dynamic system is broken up into individual subtasks that are distributed among the local controllers. The general goal of our research is to obtain a fundamental understanding of the structural aspects of decentralized and distributed control and to develop corresponding methodologies for optimum distribution of tasks among available individual controllers, yielding high nominal performance, good disturbance rejection, and robustness in the presence of modeling uncertainties. For the latter, special attention will be given to systematic design methodologies for low-order dynamic controllers, and controllers with structural constraints, in order to meet engineering specifications such as the sampling rate, computation time, and active/passive decomposition based on response characteristics of employed materials.

The problem of optimum distribution of control tasks among individual local controllers also involves, at a higher level, the optimum design of information and data transmission links for control and decision-making purposes that will support the requisite (possibly asynchronous) communication among the control stations. Such designs, under physical implementation constraints, pose challenging deterministic and stochastic optimal control problems whose solutions require the development of new methodologies and novel analytical and numerical techniques. Pursuing this will be another objective of our research.

SUMMARY OF RESEARCH:

During this period, one topic of concentration has been worst-case design problems, particularly the derivation of H^{∞}-optimal controllers for disturbance attenuation in both discrete and continuous-time systems, under different information patterns. In all cases we relate the H^{∞}-optimal control problem to a particular linear-quadratic differential/dynamic game, with the quantity of interest being the upper value of the game.

For the discrete time, finite-horizon problem, we have shown that an optimal (minimax) controller exists (in contrast with the continuous-time H^{∞} control problem), which can be expressed in terms of a generalized (time-varying) discrete-time Riccati equation. The existence of an optimum also holds in the infinite-horizon case, under an appropriate observability condition, with the optimal control, given in terms of a generalized algebraic Riccati equation, also being stabilizing. In both cases, the corresponding worst-case disturbances turn out to be correlated random sequences with discrete distributions, which means that the problem (viewed as a dynamic game between the controller and the disturbance) does not admit a pure-strategy saddle point. We have also obtained results for the delayed state measurement and the nonzero initial state cases. Furthermore, we have formulated a stochastic version of the problem, where the disturbance is a partially stochastic process with fixed higher order moments (other than the mean). In this case, the minimax controller depends on the energy bound of the disturbance, provided that it is below a certain threshold.

For the continuous time problem, on the other hand, when the controller has access to the current value of the state, the optimum attenuation level is determined by the nonexistence of a conjugate point to a particular Riccati differential equation (RDE) in the finite horizon and by the nonexistence of a positive definite solution to an algebraic Riccati equation (ARE) in the infinite horizon case. In contradistinction with the discrete-time case, however, a corresponding optimal controller may not exist. There exist suboptimal linear feedback controllers ensuring attenuation levels arbitrarily close to the optimum ones.

Under sampled-data measurements, a set of additional RDE's whose boundary conditions are determined by the solution of the perfect state RDE play a key role in the determination of the optimum attenuation level. A controller that achieves a performance level arbitrarily close to the optimum is again a linear feedback rule that uses the most recent sampled value of the state. For the infinite-horizon version, the optimum attenuation level is determined by one ARE and one RDE, with the latter determined on the longest sampling interval. The same conditions apply to the infinite-horizon delayed state measurement problem as well, even though the near-optimal controllers in this case have completely different structures.

We have also studied a class of minimax filtering, prediction, and smoothing problems for linear time-varying systems in both discrete and continuous time by making use of the saddle point of a particular quadratic game. The main structural difference between the performance index here and those adopted in the study of the problems discussed above is that here the "gain" is from the disturbance(s) to the pointwise (instead of cumulative) output (which in this case is the estimation error). This difference in the cost functions leads to an important structural difference in the solutions, in that for the class of problems studied here the minimax decision rules (estimators) can be obtained without computing the associated minimax attenuation levels—a feature the controllers discussed above did not have. As a result, here the minimax estimators and the associated performance levels have been determined independently, with the former being Bayes estimators with respect to Gaussian distributions (which then readily leads to the Kalman-type recursive structures), and the latter (that is, the minimax disturbance attenuation levels) determined from the solutions of some related linear quadratic (indefinite) optimal control problems.

Research on robust and reliable control has concentrated on the development of efficient approaches to design of reliable centralized and decentralized control systems, for which stability and performance are guaranteed not only for the normal operating mode when all sensors and actuators are operational but also in selected failure modes, when some sensors or actuators can fail. The developed designs guarantee an H_{∞} norm bound from noise inputs to the regulated outputs for

normal operation as well as for all admissible failure modes. This allows an acceptable level of degradation of system performance to exist until the failed sensor or actuator can be replaced, or until the controller can be reconfigured.

In the case of sensor outages, design equations have been developed for the case when the failed sensor channel transmits no signal to the controller and also for the case when the measured signal is lost but the transducer still injects measurement noise into the closed-loop system. In the case of actuator failures, the case when an apriori bound on the control energy to noise energy ratio is guaranteed only for those controls that remain operational after a failure has been considered, as well as the case when this ratio is bounded even for control components that fail. This insures the use of an open-loop stable controller. Decentralized reliable controllers have also been developed for the case when certain control channels can fail. Both continuous-time and discrete-time problems have been studied.

Efforts on the development of efficient methods for the design of low-order controllers were concentrated on the study of the properties of the Frobenius-Hankel (FH) norm. This norm is of particular interest because it depends explicitly on both the gain (i.e. magnitude) and the phase of the transfer function of a linear time-invariant system, as opposed to other extensively used norms, such as the H_2 and the H_∞ norm, which depend solely on the magnitude of the transfer function.

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WORK UNIT NUMBER 15

TITLE: Sensor-Array Imaging of Dynamic Scenes

SENIOR INVESTIGATORS:

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SCIENTIFIC OBJECTIVE:

In some sensor-array imaging systems, many spatially disparate sensors are used to sample the input signal; in others, a single sensor is moved from one spatial location to another. Important types of sensor arrays include synthetic aperture radar (SAR) X-ray computer tomography (CT), and scanning laser range-finders. In many applications, during the total data collection period, the scene being imaged changes with time due to motion so that the sensors do not "see" the same scene from every spatial or angular vantage point. For example, this occurs in SAR imaging of moving vehicles or in CT imaging of the beating heart.

The objective of our research program is to study the basic issues in using sensor arrays to image dynamic scenes, including the detection, estimation, and correction of motion, and the optimal design of image acquisition systems. In our study, we are examining both the single-frame and the multiple-frame cases. We are mainly interested, however, in the case where the amount of object motion or scene change is significant during the time interval used to collect one image frame, not in the case where the effects of the object motion within a single frame can be neglected.

In the case of small motion during the data collection interval, the effect of the motion is to blur the desired image For this case, we hope to quantify and characterize the image degradation resulting from scene motion and to develop algorithms to detect the moving parts of the scene and correct for the blurring. In the case of large motion, our aim is to detect and track moving targets and to estimate their motion parameters. In both the small-motion and the large-motion cases, we are also interested in designing optimal acquisition schemes to facilitate the tasks of motion detection, estimation, and correction.

SUMMARY OF RESEARCH:

During the past year, our research has focused on several facets of sensor-array imaging of moving scenes: 3-D motion estimation, interpolation, time-sequential image acquisition, tomographic reconstruction, and time-frequency waveform synthesis. In the area of 3-D motion estimation, we have investigated methods based on both visual input (image sequences from CCD cameras) and SAR-type input signals. In the first case, we have developed techniques for 3-D motion estimation by tracking point and line features and have applied these techniques successfully to real-world image data [1,2]. In the second case, some interesting preliminary results have been obtained [3]. We have developed an algorithm for estimating the rotation speed based on SAR-type signals from a point source that is orbiting around a fixed axis. There are three phases in our algorithm. In the first phase, the preprocessing step, we use *a priori* information to obtain a range of possible rotation speeds. Accordingly, in the second phase we can construct images using different rotation speeds. In the third phase, we compute the variance of the distribution of each of the reconstructed point sources. The correct reconstructed image has the smallest variance, while other images would have larger variances due to the nonlinear effects induced during the reconstruction phase. We have applied this algorithm to a number of simulated data and satisfactory results are obtained. With this algorithm, we can estimate the rotation speed with error less than 2% in more than 85% of the cases. The average estimation error is less than 0.5%, and the largest error is only 5.7%.

Our work on the general interpolation problem is motivated by the fact that many sensor array systems provide data that must be interpolated either spatially or i frequency as part of the image formation process. Furthermore, in the imaging of time-varying distributions by sensor arrays, a nonuniform sampling pattern in both space and time is created, requiring the interpolation in both the temporal and spatial dimensions.

In [4] we studied the properties of minimax-optimal interpolation, where the worst-case performance of the interpolator over an allowable signal class was optimized. We showed that for a broad class of interpolation problems the minimax-optimal interpolator is invariant to the error norm that is chosen as a performance criterion for the optimality of the algorithm. This result has a broad range of applications, particularly in situations where it is difficult to agree on a particular norm as a relevant performance measure, such as in speech and image processing.

Ongoing work involves a comparison between minimax-optimal and conventional low-pass interpolation for uniformly spaced data. Such comparison is of interest, since low-pass filters, which are not optimal for a finite number of data points, are often used in practice. We analyzed the performance of both interpolators in the mini-max sense and developed intermediate interpolators that trade-off performance for computational simplicity. A publication on this subject is in preparation.

In other work on interpolation, we have analyzed a fast, chirp-z transform approach to interpolation between two uniform grids [5]. This method can be employed even if the sampling rate ratio between the two grids is irrational. The method requires 0(NlogN) multiplications when the input grid has N samples. In this work, we have characterized the interpolation problem in the Fourier domain and then derived the chirp-z interpolation algorithm. Through computer simulation, the proposed algorithm was compared with some existing approaches to interpolation in terms of computational complexity and accuracy and was shown to perform extremely well, especially for digital signals with wide bandwidths.

We have also addressed the problem of reconstructing a bandlimited signal from a set of nonuniformly spaced samples, with particular emphasis on a method due to J. L. Yen. A new simple proof for the derivation of Yen's interpolation formula was developed [6]. The interpolating process was then modeled as a linear time-varying system and analyzed in the frequency domain by means of its bifrequency transmission function (BFTF). It was proved that Yen's interpolator can be obtained as a special case of an optimal frequency-domain design of its BFTF using a weighted least-squares

criterion. A practical interpolator, based on Yen's method, was considered for situations where the number of samples is large or infinite and the original Yen interpolation formula is inapplicable. The performance of this modified Yen interpolator was compared with other commonly used interpolation methods in terms of achievable S/N and was shown to perform significantly better.

Motivated by the need to sequentially acquire the data from a time-varying scenes, and by the encouraging results of our study of optimal tomographic acquisition and reconstruction of time-varying distributions, we have expanded our study to the general problem of time-sequential sampling. We have obtained a readily computable minimax-performance measure for time-sequential sampling and upper bounds on the performance of such sampling, which provide a characterization of when unconventional sampling schemes are useful. In a different direction, we are studying efficient iterative algorithms for the optimization of the optimum time-sequential sampling pattern for a given signal class. Preliminary results of this work will be presented in [7].

We have continued our investigation of tomographic imaging of time-varying distributions. The tomographic model for SAR imaging provides a convenient mathematical framework for the analysis of many facets of the imaging problem, and results obtained in this framework are generic enough to be applicable to many other medical, industrial, and scientific problems. As in [8], we addressed the case when the temporal variation during acquisition of the data is high, precluding Nyquist rate sampling, and aperiodic, precluding reduction to the time-invariant case by synchronous acquisition. In [9] we generalized the techniques of [8] to find the optimal angular sampling order for a broad class of images, demonstrating a reduction in sampling rate to 1/4 Nyquist, with no significant degradation of reconstruction quality, for an *arbitrary* test image. Work is in progress to realize much greater improvements, which are theoretically possible. These sampling rate reductions address a fundamental limiting factor in the imaging of time-varying data. Application of these techniques are foreseen in SAR imaging, X-ray computer tomography, and magnetic resonance imaging. A journal paper on this work is in preparation.

Range-Doppler radar has long been used to estimate the range and velocity of a moving target. Furthermore, a 2-D range-Doppler image can be produced by utilizing a bank of matched filters. The performance of such systems is determined by the ambiguity function of the transmitted waveform, which characterizes the range and Doppler resolution trade-off. In [10] we showed that the optimal solution for least-squares ambiguity function synthesis in the continuous time-frequency domain is found as a solution to a homogeneous Fredholm integral equation of the second kind. We showed that the least-squares cost function is not convex, making it difficult to use standard optimization algorithms for weighted least-squares synthesis problems. An exact expression for the continuous ambiguity function of a time-limited waveform in terms of the discrete ambiguity function of the same waveform was given and the resulting aliasing problem was investigated. The least-squares synthesis of ambiguity functions for time-limited waveforms in the discrete time-frequency domain was also solved. A practical suboptimal design algorithm was devised, which specifies all but finitely many frequency samples as zero. Also, a relation was given between discrete Wigner distributions obtained using samples taken at the Nyquist rate and at twice the Nyquist rate, and it was shown that the corresponding discrete Wigner distribution synthesis can be performed using essentially the same algorithm proposed for ambiguity function synthesis. It is expected that these results will be useful in designing waveforms for radar imaging of moving targets and also for segmenting nonstationary signals whose components overlap in both time and frequency.

In preparation for the application of model-based techniques for the resolution of moving targets from array data, we have directed some of our work to the fundamental problem of parameter estimation of superimposed signals in noise. We have derived [11] a compact close-form Cramer-Rao bound expression for this problem for real or complex signals with vector parameters. We have studied [12,13] the effect of the correlation structure of the signals on the Cramer-Rao bounds and have determined the best and worst cases. These results are useful for studying the fundamental limits on the resolution of close targets and for the design of minimax signal acquisition and estimation procedures. Addressing the computationally difficult problem of maximum likelihood parameter estimation for multiple signals, we have developed [14,15,16] an efficient algorithm for

finding a globally optimal solution, whose computational requirements are linear in the number of signals, rather than exponential as in the case of exhaustive search. The analysis [17] of these algorithms indicates excellent performance.

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WORK UNIT NUMBER 16

TITLE: Topics in Survivable Communication Networks

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SCIENTIFIC OBJECTIVES:

The general objective of this unit is to improve the state of the art in survivable communication networks by investigating some critical issues in communication network design and performance. A better understanding of the fundamental trade-offs between communication efficiency and survivability will be obtained, and improved modulation and coding schemes, receiver processing techniques, and network protocols will be developed for use in communication networks that will be subjected to jamming, fading, and loss of resources.

Improved adaptive coding techniques and adaptive protocols for meteor-burst communication will be developed, and the role of meteor-burst communication links in mixed-media communication networks will be investigated. New methods for modulation, transmission, and coding will be obtained for use in frequency-hop communication over HF and other channels with fading, partial-band jamming, and various forms of radio-frequency interference. Synchronization procedures for spread-spectrum signals will be investigated, with particular emphasis on channels with multiple-access interference and fading. Finally, a better understanding of network-directed electronic countermeasures (ECM) will be sought, particularly those concerned with thwarting traffic analyses and operating under emission control.

STATE OF THE ART:

Survivability is perhaps the most important requirement for modern military communication systems and networks, yet much remains to be done to provide it for the communication environments that will be encountered in the future. The problem is complicated by the large number and wide variety of potential threats present in a battlefield environment, including aggressive electronic countermeasures that range from jamming to sophisticated attacks against network protocols. The RF environment for modern military communications is corrupted by a large number of non-Gaussian sources of interference including other-user interference and intelligent jammers. The potential disruption of communication by such interference, along with the possible loss of some network resources, can lead to a loss of network connectivity, particularly in networks with high mobility or those with only a small number of communication platforms in a given region. The communication and synchronization capabilities that are needed to reconfigure a network under stress

are difficult to ensure. While spread-spectrum signaling, in conjunction with diversity transmission and error-control coding, has been quite successful in providing a certain level of anti-jam (AJ) and low-probability-of-intercept (LPI) capability, there remains a great need for improved synchronization methods for acquisition in the presence of interference, adaptive signaling and coding methods for meteor-burst channels and other time-varying channels employed by military systems and networks, and novel network-based ECCM techniques.

SUMMARY OF RESEARCH:

Our research on transmission protocols and adaptive techniques for meteor-burst communications has resulted in two journal articles that will be published in the very near future. Our paper on the use of incremental redundancy in a type-II hybrid ARQ protocol [3] demonstrates that larger throughput can be achieved with this protocol than with either fixed-rate type-I hybrid ARQ or ARQ without forward error correction. Our paper on variable-rate hybrid ARQ [4] shows that the use of variable-rate coding in a type-I hybrid ARQ system can also improve throughput over fixed-rate type-I hybrid ARQ and ARQ without forward error correction.

We are investigating the use of decision-theoretic techniques for obtaining side information in frequency-hop communications with partial-band interference. The side information is used to erase unreliable symbols in order to improve the performance of the error-control coding system. In [8], the performance of a frequency-hop system with Reed-Solomon coding and Bayesian erasure insertion is analyzed for channels with both partial-band and wideband Gaussian noise. The resulting performance is compared with that of receivers that do not erase symbols and with receivers that erase all of the symbols affected by the partial-band interference. Large gains in performance for the Bayesian method are demonstrated. It is also of interest to apply this approach to a frequency-hop multiple-access system in order to erase unreliable symbols affected by multiple-access interference. Work on this topic is in progress.

In recent work on direct-sequence spread spectrum, we examined the influence of the choice of the spreading sequence on the performance of differentially coherent communications over frequency-selective fading channels [10]. We found that the performance depends critically on the properties of the spreading sequence. We also showed that for a moderate range of delay spreads, sequences can be found that perform well over the entire range. These sequences are also reasonably robust with respect to the shape of the delay spectrum and the signal-to-noise ratio.

In our continuing study of acquisition in direct-sequence spread spectrum, we examined the asymptotic limits on capacity imposed by the acquisition requirements. For a passive matched filter acquisition scheme, we found that if the acquisition window is linearly related to the processing gain, the acquisition requirements limit the capacity more than the demodulation requirements [9]. We have also examined parallel schemes for acquisition of direct-sequence signals in totally asynchronous systems. Here, the signal is deemed to have been acquired if the true delay and the estimated delay differ by no more than ς where $\varsigma \leq \frac{1}{2}T_c$ and T_c is the chip duration, and the measure of performance is the probability that the error in the estimate of the delay exceeds ς. The general form of the optimal estimator (i.e., the estimator that minimizes this probability) is difficult to obtain for arbitrary values of ς but can be obtained for specific values of ς. In particular, we have obtained complete results for the important case $\varsigma = \frac{1}{2}$ and for the limiting form as ς approaches 0. The latter estimator is in fact the maximum-likelihood estimator (MLE), and we have shown that the MLE is also the solution to a least-mean-square curve fitting problem in which one attempts to fit the known autocorrelation function of the sequence to the observations. Another curious property of the MLE is that even though the actual delay is assumed to be a continuous random variable, the MLE estimate of the delay is a mixed random variable. Thus, there is a nonzero probability that the MLE will be an integer multiple of the chip duration T_c. Other schemes that we have examined include those for which $\varsigma = \frac{1}{2}$ and for which the estimator is restricted to be of the form $(k + \frac{1}{2})T_c$. The restricted optimum estimator and the restricted locally optimum estimator have been obtained. Finally, we have evaluated the performance of all these schemes by various means. We have derived

bounds and approximations for the error probability of all these schemes and have also used Monte Carlo simulations to compare the actual performance with our analytical approximations and bounds. Detailed results are given in [12].

We have recently made progress on the problem of thwarting traffic analysis in a radio network. This problem, which is in the broad area of network-based electronic counter counter-measures (ECCM), is to prevent an eavesdropper from deducing end-to-end traffic patterns. Even if packet headers and data are securely encrypted (as we assume), an eavesdropper can potentially determine the identity of a command node, anticipate and jam acknowledgments, follow messages across the network, or deduce the original sender of a message. *Ad hoc* solutions involve sending dummy packets and randomizing acknowledgement times.

The more systematic approach we take is to choose transmission schedules independently of the end-to-end traffic demand. The eavesdropper then learns nothing about the underlying traffic flow by monitoring the sequence of transmissions. A fundamental question on which we have made progress is to determine the resulting loss in throughput, or slowdown, that results when such counter counter-measures are used. For example, consider a spread spectrum system with perfect capture. We found that there are simple node transmission schedules such that, for any traffic demand, the throughput is reduced by less than a factor of four over what the throughput would be if the link transmission were adjusted as a function of the traffic demand. Moreover, a simple formula for calculating the worst-case slowdown is given when the traffic routes are specified along with the demand.

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WORK UNIT NUMBER 17

TITLE: Adaptive Signal Processing

SENIOR INVESTIGATORS:

K. S. Arun, Research Assistant Professor
W. K. Jenkins, Research Professor
D. L. Jones, Research Assistant Professor
H. V. Poor, Research Professor

SCIENTIFIC PERSONNEL AND TITLES:

M. Aung, Research Assistant
R. G. Baraniuk, Research Assistant
S. Dharanipragada, Research Assistant
A. H. Hull, Research Assistant
J. Strait, Research Assistant
V. Veeravalli, Research Assistant

SCIENTIFIC OBJECTIVE:

The overall scientific objective of this unit is the development of techniques for the extraction and/or enhancement of time-varying (nonstationary) signals from additive noise. The characteristics of signals encountered in practice are often time-varying; for example, the ocean acoustic channel and the signals of interest there are all strongly time-varying, as are most high-speed communication channels of interest to the military. Nonstationary signal behavior often severely limits the performance of conventional signal analysis tools, such as FFT-based spectral analysis and narrow-band bandpass filtering. In time-varying situations, since the variation with time is rarely known beforehand, adaptivity is the key to effective system performance. In this research unit, we are developing adaptive approaches for processing several important classes of time-varying signals and algorithms to extract relevant information from nonstationary signals. We expect that these algorithms will have performance comparable to that of conventional techniques applied to stationary signals.

Both parametric and nonparametric approaches are being investigated in this project. For narrow-band signals with time-varying frequencies, high-resolution parametric methods based on singular value decomposition are under study. For wide-band signals, we are investigating non-parametric methods such as time-frequency analysis, as well as high-resolution parametric methods based on slowly varying ARMA and AR models. For the tracking of these time-varying system models, adaptive FIR and IIR filtering methods will be investigated. The objectives are to develop computationally efficient adaptive time-frequency representations and new adaptation algorithms and adaptive filter structures that are computationally efficient for real-time applications, are robust, and are suitable for short wordlength VLSI circuit implementation.

SUMMARY OF RESEARCH:

During the last year our JSEP-supported research concentrated on four specific topics that are judged to be of fundamental importance in adaptive signal processing: (i) the study of new adaptive algorithms and digital filter architectures for both one- and two-dimensional adaptive filters with improved learning characteristics and reduced computational complexity; (ii) the study of adaptive filters with fault tolerance; (iii) computationally efficient signal-dependent time-frequency representations and parametric models of time-varying signals; and (iv) detection and tracking of superimposed narrowband signals. Brief descriptions of progress in these four areas follow.

(i) New Adaptive Algorithms and Digital Filter Architectures with Improved Learning Characteristics and Reduced Computational Complexity

The rapid advancement of digital microcomputing devices has fueled a sustained interest in adaptive filtering and has led to rapid applications in new fields. Pioneering efforts in communications brought early success for adaptive filtering in favorable environments, e.g., those with high signal-to-noise ratios and slowly varying channel characteristics, such as in voice-grade telephone channels. The complexity of adaptive filters in such applications is moderate, and general purpose computing devices now render their implementation elementary.

The scope of applications for adaptive filters has now broadened into areas requiring extremely high-order filters with more than one thousand taps to accurately model unknown phenomena. Examples requiring such adaptive filters include acoustic echo cancellation and satellite channel equalization. Other new applications require rapid convergence to track highly variable environments. The equalization of mobile telephone channels presents one such environment. The demand for increasingly higher data rates through twisted-pair lines will continue to place greater demands on adaptive equalization techniques. Some specialized tasks required for defense purposes even use filters requiring millions of taps. This trend toward higher filter order and more demanding environments will be the driving force behind adaptive filter algorithm development.

In our recent research we have introduced a family of rapidly converging IIR adaptive algorithms with O(N) computational complexity, where N is the filter order. By observing the similarity between the numerical solution of partial differential equations and the IIR adaptive filtering problem, results from the solution of systems of sparse linear equations may be employed. In this novel formulation the identification problem of the IIR coefficients separates into two sub-problems, each of which may be solved by application of fast adaptive FIR techniques. In recent work, the method of Preconditioned Conjugate Gradients (PCG) was proposed for solving the problem of high-order adaptive filtering. When considered as an iterative algorithm, the PCG is asymptotically efficient, suggesting that its primary use would be in applications requiring very high-order adaptive filters.

In the area of 2-D adaptive filters, a new 2-D filter architecture was developed based on a concept similar to a 1-D joint process estimator (JPE), which consists of an adaptive lattice prediction error filter followed by a set of adaptive "output" coefficients. The 2-D JPE is made up of a 2-D lattice structure followed by a generalized arrangement of output coefficients that allow the 2-D JPE to match an arbitrary unknown 2-D system. This new 2-D adaptive structure was shown to offer convergence rate improvement over a direct form 2-D LMS adaptive filter. One drawback of the proposed 2-D JPE is that it exhibits a rather large minimum MSE. An analysis of this effect, which provides an overall upper bound for the noise floor, was presented for the new 2-D structure. Computational considerations involved in implementing the new 2-D JPE were also addressed.

An important application of 2-D adaptive filtering is in LPC coding of images. In this application a 2-D adaptive digital filter is used as a linear predictor to estimate image pixels that

lie in the "future" of the current pixel location. The predicted pixel value is subtracted from the actual pixel value, and the difference, referred to as the prediction error, is encoded as the representation of the pixel. The prediction errors are minimized at each step by adapting the coefficients of the prediction filter. In some applications a simple 1-D FIR is used to do the prediction along the 1-D raster scan direction. In other cases a true 2-D FIR filter has been used. Our current research considers the use of various 2-D adaptive filter architectures for this application. The objective is to achieve high-quality prediction with rapid learning characteristics, while minimizing the amount of computation that must be done at each iteration. It is expected that an improvement in the characteristics of the 2-D adaptive prediction filter will result in a more effective image compression algorithm.

(ii) Adaptive Filters with Fault Tolerance

Since adaptive systems, such as adaptive echo cancellers, adaptive equalizers, and adaptive controllers, are capable of adjusting their own system parameters to reduce a specified error criterion, it is expected that whenever a hardware failure occurs that increases the error, the system will attempt to compensate for this failure by further adjusting the system parameters to reduce the error to the greatest extent possible. This research investigates ways to design filters with enough degrees of freedom so that the adaptive process can eliminate the ill effects of a failure through adaptive self-adjustment.

The analysis in our most recent work in this area focused on two specific finite impulse response (FIR) adaptive structures: (1) the conventional time domain least-mean-squares (LMS) adaptive filter and (2) the transform domain least-mean-squares (TDLMS) adaptive filter. A fault-tolerant adaptive filter structure was presented that is formed from a parallel combination of a time domain LMS filter and a TDLMS filter, and it was shown how the redundant parameters in this hybrid structure can take over the function of other parameters that become faulty through "stuck-at faults." It was also shown that the orthogonal transformation that is inherent in the TDLMS subsystem provides a convenient mathematical framework in which to achieve various design goals through the selection of an appropriate transformation matrix. The hybrid filter is generalized into a structure that consists of two TDLMS filters with different orthogonal transformations connected in parallel. Finally, it was shown how the deadband effect in fixed point arithmetic helps to stabilize the adaptation in the over-parameterized case, and saturation arithmetic is proposed to further stabilize the adaptation process.

The subject of adaptive fault tolerance is not yet a very well understood subject, and a great amount of future research is needed to fully develop these concepts. It is intended that this initial work in adaptive fault tolerance will be continued during the coming year.

(iii) Computationally Efficient Signal-Dependent Time-Frequency Representations

We have completed the development of a computationally efficient, signal-dependent time-frequency representation that automatically suppresses cross-terms while minimizing auto-component distortion. The method designs an optimal signal-dependent kernel by solving a specialized linear program [6,9]. An extremely efficient algorithm for computing the optimal kernel has been developed, with a computational cost of the same order as fixed-kernel time-frequency representations. Adaptivity of the kernel is thus obtained with no increase in the order of the computation. We have also shown that the optimal kernel necessarily takes on values of either unity or zero. The sharp edges in the kernel can lead to truncation artifacts, or "ringing," in the time-frequency representation. Another optimal design procedure using radially Gaussian kernels, which are inherently smoothed, has been developed to counter this problem. There has been substantial early interest in these techniques, and programs implementing these new algorithms have been distributed to several defense contractors for evaluation of the algorithms for sonar applications.

Continued work in efficient polynomial modeling of phase has yielded improved methods which essentially achieve the Cramer-Rao bound for signal-to-noise regimes above a threshold. Both O[N] and O[N log N] methods have been developed. The threshold of these methods appears to be only three to four decibels above that of the (very expensive) minimum-mean-squared-error estimator, and several decibels lower than the threshold of current methods.

An efficient algorithm for computing dense samples of the continuous wavelet transform and the broadband ambiguity function has been developed. The fast algorithm uses the chirp Z transform to efficiently implement both the wavelet scale change and convolution with the signal in the frequency domain. The computational cost is O[MNlogN], where M is the number of scale values, and N is the number of samples in the signal.

(iv) Detection and Tracking of Nonstationary Superimposed Narrowband Signals

Detection and estimation of multiple narrow-band components in a time-series is a difficult signal-processing problem that shows up in many applications. We have been investigating a parametric approach to the problem and examine an algorithm based on singular value decomposition to estimate and track the parameters. Each narrowband component is modelled as a sinusoid with slowly varying amplitude and frequency. In this research period, we developed bounds for the distance of a matrix constructed with the noise-free data from a matrix whose rank is equal to the number of signal components. We hope to use these bounds to predict the performance of the tracking algorithm when prior knowledge of rate of change is available. We are currently working on developing fundamental, theoretical performance bounds using Cramer-Rao-like inequalities.

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WORK UNIT NUMBER 18

TITLE: Initiatives in Electronics Research

PRINCIPAL INVESTIGATOR:

W. K. Jenkins, Research Professor and CSL Director

SCIENTIFIC OBJECTIVE:

The objective of this unit is to provide discretionary funds to the Director for support of new initiatives on basic problems of electronic materials, devices, and systems in a timely manner and to provide early start-up funding of projects that present immediate opportunities of high scientific promise. These discretionary funds are an important feature of the JSEP program because they support exploratory work on new topics, provide matching equipment funds in the laboratory, and support promising new faculty where appropriate.

SUMMARY OF RESEARCH:

The University of Illinois EpiCenter, which was described in considerable detail in last year's JSEP Progress Report, has been in full scale operation during the second year of the present JSEP grant. The EpiCenter is a $6 million facility located in the east wing of the Coordinated Science Laboratory that is jointly sponsored and managed by the Coordinated Science Laboratory, the Materials Research Laboratory, and the Microelectronics Laboratory. In addition to its initial investment of over $500,000 in the EpiCenter, CSL contributes approximately $42,000 annually to the center's operating fund that was budgeted during 1991 at a total level of $115,000. During the second year of the JSEP contract (October 1, 1990 through September 30, 1991) CSL will contribute approximately $25,000 of the JSEP Director's Fund toward the operation of the EpiCenter, with the remaining $15,000 coming from general CSL indirect cost returns. The operating budget pays the salary of a full-time Research Engineer who maintains the facility and supports certain common facility expenses incurred for installation and maintenance of the equipment. The major costs for operating the EpiCenter are charged as direct expenses to the individual research programs that make use of the EpiCenter facilities.

During the second year of the current JSEP grant, $15,000 was allocated from the JSEP Director's Fund to cost share the purchase of a Janis Optimag liquid helium dewar that is needed to support the work of Professors Adesida and Leburton in Unit 7, "Electronic and Transport Properties of Ultra-Low-Dimensional Semiconductor Structures." This new piece of equipment will make it possible to achieve accurate low-temperature measurements on "quantum wires" that are being fabricated and characterized in the research of this unit.

At the time of the last Illinois three-year JSEP review in June of 1989, a Supplementary Unit entitled "A Study of Quantum-Well Lasers and Novel Optoelectronic Devices," proposed by Professor S. L. Chuang, received an outstanding review but could not be funded as part of the regular JSEP contract due to the lack of new funds for supplementary work. Subsequently, Professors Jenkins and Chuang worked with Dr. Larry Cooper of ONR to have this project funded as a new individual PI grant under Dr. Cooper's initiative program in optoelectronics. In order to initiate this program, Professor Jenkins pledged $25,000 of start-up monies from the JSEP Director's Fund for the period May 1, 1990 through April 30, 1991. Additional support in the amount of $15,000 has been provided by the Director's Fund for the period May 1, 1991 through September 30, 1991. This continuing project (Unit 20), which is now receiving increasing support on its own merit, is an

excellent example of the leverage that can be provided by the Director's Fund in order to initiate new projects in a timely manner when appropriate opportunities arise.

In 1983 Professor Bill Hunsinger and his Ph.D. student Michael Hoskins invented a new surface acoustic wave device concept that has since become known as Acoustic Charge Transport (ACT) device technology. The early research that led to this development was supported in part by JSEP. Professor Hunsinger then formed a start-up company in Urbana, called Electronic Decisions, Inc., (EDI), to develop and eventually commercialize ACT technology. During the last year, an opportunity arose in which the State of Illinois and DARPA jointly granted the Coordinated Science Laboratory $450,000 to conduct basic research in systems level applications of ACT devices and to establish an ACT Signal-Microprocessor Applications Laboratory at CSL. In particular, the use of ACT devices in wide bandwith radar, communications, and sensor array systems is being investigated. In order to initiate this project, the Coordinated Science Laboratory contributed $25,000 in equipment funds to leverage the State funds and to get the project started. Of this total, $15,000 was pledged from the JSEP Director's Fund to purchase PC's that are used to control the hardware development modules that are provided by EDI as part of their support for this project. This is another example of how the Director's Fund provides flexible resources that allow the Director to pursue unique research opportunities in a timely fashion.

The remaining $30,000 from the second-year budget of the Director's Fund has been pledged to support start-up activities and partial summer support for Assistant Professors Yoram Bresler, Douglas Jones, and Leslie Allen. Professors Bresler and Jones are participating in the regular JSEP program (Units 15 and 17, respectively), and their own research programs have developed nicely over the last three years. It is expected they will be self-supporting in the future and will need no further assistance from the Director's Fund. Professor Leslie Allen joined CSL in the fall of 1990 as a member of the faculty in the Materials Science and Engineering Department. He is preparing a proposal for supplementary support, and it is our hope that he can eventually become a regular participant in our JSEP program.

WORK UNIT NUMBER 20
(Supplementary Unit Funded Partially by JSEP and Partially by an ONR Individual PI Grant)

TITLE: A Study of Quantum-Well Lasers and Novel Optoelectronic Devices

SENIOR INVESTIGATOR:

S. L. Chuang, Associate Professor

SCIENTIFIC PERSONNEL AND TITLES:

C. Y. P. Chao, Research Assistant
P. J. Mares, Research Assistant

SCIENTIFIC OBJECTIVE:

The general objective is to investigate, theoretically and experimentally, the electrical and optical properties of semiconductor quantum wells and their applications to lasers and other optoelectronic devices. In this report, we focus on the electroabsorption effects in quantum wells and the modeling of both electrooptical modulators and self-electrooptic effect devices (SEED's). We have developed two models for the electroabsorption effects in quantum wells (quantum confined Stark effect). In one model we include excitonic behavior via the variational method, while in the other we include the realistic band structure for both the conduction and valence subbands and then calculate the field-dependent absorption spectra by solving the exciton effective mass equation directly in momentum space. In the latter approach, the absorption due to the exciton continuum states, as well as that due to the bound states, can be obtained accurately without any adjustable parameters. We have also set up our optoelectronics laboratory, and our experimental investigations, including differential absorption spectroscopy of multiple quantum well structures, are under way.

SUMMARY OF RESEARCH:

I. Electroabsorption Effects in Semiconductor Quantum Wells

Modeling the electroabsorption effects in semiconductor quantum wells requires an accurate and efficient algorithm to solve the exciton effective mass equation. A comprehensive model should, at least, include: the different effective masses for the well and barrier, the valence band mixing effects, the Coulomb coupling between different subbands, the conduction band nonparabolicity, and the mismatch between dielectric constants of the well and the barrier. Further, the exciton bound states and the continuum states should be treated on an equal footing. Most of the previously published work is based on variational calculations and, therefore, is unable to accurately account for the exciton continuum states. Consequently, one of our approaches is to solve the exciton equation, in the form of an integral equation, directly in momentum space using a modified Gaussian quadrature method [6]. We are using this model to investigate the effects of valence band mixing on multiple quantum well structures.

Valence band mixing is a subject of great interest to scientists and engineers in the field of quantum well electronics. Theoretically, it is well understood via the Kohn-Luttinger formalism. However, the many attempts to unambiguously demonstrate experimentally the effects of valance

band mixing have so far been inconclusive. Recently, in cooperation with Dr. Fox at Oxford University and Dr. D. A. B. Miller et al. at AT&T Bell Labs, we have developed a theoretical model to explain the experimentally obtained photocurrent spectra for various GaAs/AlGaAs multiple quantum well samples. The spectra show clearly resolved anticrossings between the heavy- and light hole-exciton transitions (Fig. 1a and 1b). The anticrossings indicate that the heavy- and light-hole subbands of adjacent wells are strongly coupled together when they are brought into resonance by an externally applied electric field. These observations cannot be explained by the parabolic band model that ignores such coupling, while our calculations incorporating valence band mixing fit the experimental data very well for all the samples. To the best of our knowledge, our model is the first to successfully explain this anticrossing behavior. Some of our results are shown in Fig. 1c. One important consequence of this mixing is that resonant tunneling between the heavy holes and light holes becomes possible. Therefore, the hole tunneling time, which is critical to the operating speed of quantum well devices, can be much faster than previously expected.

II. Self-Electrooptic Effect Devices: Controlling Light by Light

A self-electrooptic effect device (SEED) is a hybrid optoelectronic device with optical inputs and optical outputs. It is optically bistable and can thus function as an optical switch. A SEED consists of a multiple quantum well (MQW) p-i-n diode connected in series with a bias source and a load. The key to the SEED concept is the p-i-n diode that makes use of the strong electroabsorption effects of MQW structures (quantum confined Stark effect) and that functions simultaneously as a photodetector and as a modulator. In a SEED, the electrical circuit is responsible for the manner in which a change in photocurrent changes the voltage across the device. However, it is the photocurrent passing through the electronic circuit that changes the voltage across the modulator. The voltage across the modulator then affects the absorption of light by the modulator, which in turn causes the photocurrent to be changed. Consequently, we establish an optoelectronic feedback that is based on having a p-i-n MQW diode that will absorb progressively more of the incident light when progressively more excited by the incident light. This feedback is positive and can, under the proper conditions, lead to switching.

To realistically model the absorption spectrum, we include the effects of excitons. In our theoretical model we: (1) compute the absorption coefficient from the density matrix approach, (2) use the Kane model for the matrix elements, (3) compute the exciton binding energies using the variational method, (4) use the propagation matrix technique to determine the eigenvalues and eigenfunctions, and (5) use the depletion approximation to relate the applied bias to the electric field.

The load elements that we have considered include a resistor (R-SEED) and an identical MQW p-i-n diode (S-SEED). For the MQW p-i-n structure of Miller et al. [14], we obtained very good agreement between our theoretically computed transition energies and those experimentally determined by [14]. We also obtained a very good match between our theoretical and the experimental data of Miller et al. [15] for the response versus bias and for the transmission versus bias. Using these results, we successfully generated the input/output characteristics for the R-SEED for different bias source voltages. Our theoretical results compare very well with the experimental data in [16]. In addition, using the previously mentioned data for the response and transmission, we were able to theoretically generate the input/output characteristic of a S-SEED.

III. Band-Gap Renormalization in a Quantum Well Laser

We have obtained preliminary results on the band-gap shrinkage in quantum well lasers and in optically excited quantum well structures. The theoretical results agree very well with the experimental data. The details will be reported in the near future.

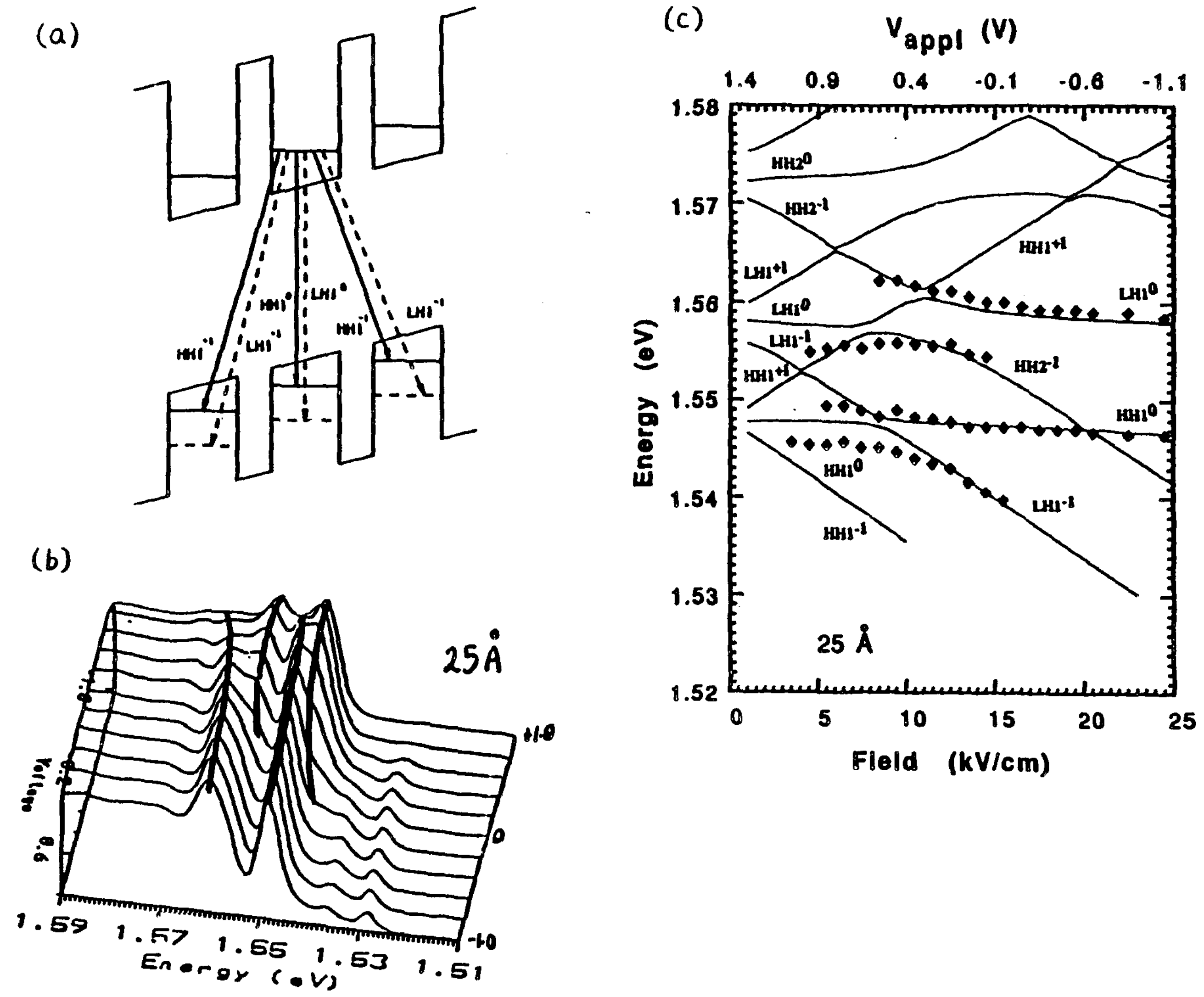

Fig 1. (a) Band diagram of the GaAs/AlGaAs multiple quantum tum wells; (b) the low temperature photocurrent (PC) spectra at various external bias voltages; (c) the exciton transition peaks resolved in the PC spectra (rhombic dots) compared with the *theoretical calculations* (*solid lines*).

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